A.C.C NEWSLETTER VOL 2 ISS 4 OCT 74

****

ACC OPEN AFTERNOON AT
THE POLYTECHNIC OF THE SOUTH BANK
LONDON SE1

ON SATURDAY NOVEMBER 16TH 1974 2-6 PM
IN THE COMPUTER UNIT 4TH FLOOR
(SEE MAP)
ALL WELCOME.....SEE YOU THERE.....

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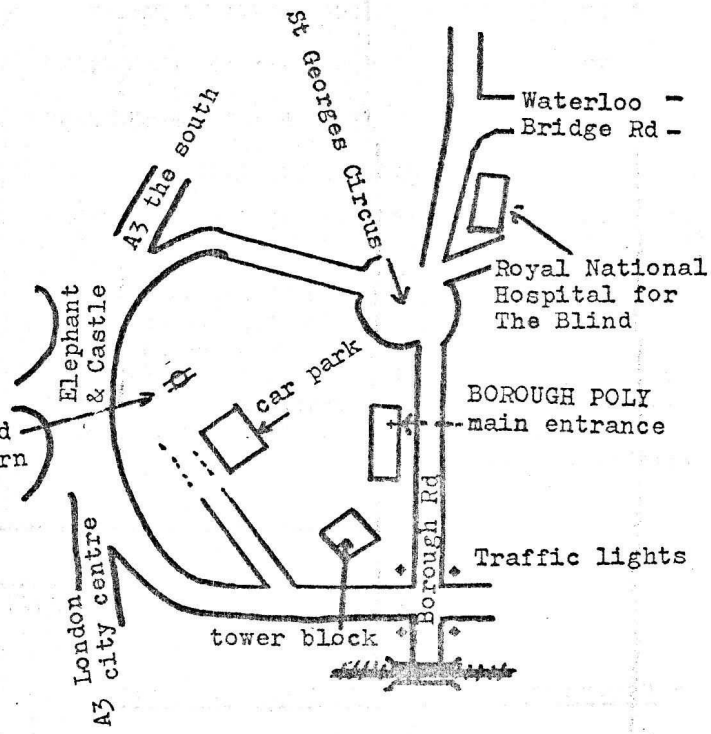


Software

Jaap Creutzberg

Random Numbers

Random numbers can be generated in many ways: spinning a roulette wheel, casting a die, counting clicks of a geiger counter etc. In each of these cases a series of real random numbers is generated, that is to say a series in which no number is in any way dependent on any other number of the series. There is no way of predicting what the next number is going to be. Nevertheless, the series as a whole will display certain predictable properties, such as a roughly equal distribution of all digits in the series.

People who use random numbers are usually more concerned that the series should have these properties than that the next number is predictable or not. Instead of throwing dice and spinning roulette wheels, random number tables are used and in these days of course computers. Chances are that the tables give a better random series than the roulette wheel! But the numbers are now no longer unpredictable. Anyone with the right set of tables knows what the next number is going to be and for this reason these numbers are known as pseudo-random numbers.

An advantage of using pseudo-random numbers is that experiments can be repeated under the same controlled conditions. A disadvantage (perhaps!) is that the tables are necessarily finite in length and if a longer series is required one must use the table again from the beginning. There is such a cycle length with any method of generating pseudo-random numbers but this can be made arbitrarily long.

A computer generated random number is usually the result of the application of a function on the last generated number. Something like this

$$R_{i+1} = f(R_i)$$

It could however be a function applied to more than one previous result.

Any method of scrambling numbers is alright as a function so long as the following conditions are satisfied within reason:

1. The series should have a long cycle length.
2. The algorithm should be fast.
3. The series should pass as many randomness tests as possible.

The first criterion can be determined experimentally by computer or in the case of arithmetic algorithms by analysis (by no means always trivial or even possible).

The second criterion depends very much on the machine used, in particular its order set. The third criterion can only be determined by experiment in the case of most tests. Which tests the series should satisfy will depend on the application, but a statistician will not easily be satisfied. Indeed, it is always possible to find a test on which a finite series fails.

A random number generator can of course be written in a high level language but since the subprogram will probably be executed many thousands of times, it is better to use an assembly language to make it as efficient as possible. This is normally no problem since the algorithms used tend to be extremely simple. Take the following algorithm as an example:

$$R_{i+1} = R_i * C+1 \text{ (modulo M)}$$

C and M have no common factors

The cycle length is M and the series generated passes a large number of tests.

It was implemented on a 1900 as follows:

```
C               371293   [= 13↑5
PV              10       [ANY OLD STARTING POINT
                         [PREFERABLY NOT 0 OR 1
START
      LDX  5    PV       [LOAD PREVIOUS RANDOM
                         [NUMBER
      MPY  5    C        [X6 = 13↑5*PV (MOD 2↑23)
      ADNC 6    1        [ADD 1 (MOD 2↑23)
      STO  6    PV       [MAKE READY FOR THE NEXT
                         [ACTIVATION
STOP                     [AND THAT'S IT
```

The value of C and particularly M were chosen to fit the 1900 hardware: word length 24 bits = 1 sign bit + 23 magnitude bits. There was thus no need to divide by 2↑23 because the truncation of the result (the 1900 leaves this in register 6) ensures that a residue modulo 2↑23 is obtained. After execution the random number is left in PV in readiness for the next activation of the code which would probably be written as a subroutine.

This algorithm would not be much good on a machine without hardware divide since the time taken by software multiplication is out of all proportion to the rest of the instructions. In this case one might try the iteration:

$$R_{i+1} = R_i + R_i \text{ (modulo M)}$$

where M is a prime of the form 8n+3 or 8n+5

The cycle length will be M and the algorithm does not involve division since $R_i < M$

There are hundreds of algorithms in use and there are many more unexplored. The thing to do is to set up a simple iteration exploiting the peculiarities of your particular machine and test the results. Do not restrict yourself to arithmetic instructions. Some machines have really weird instructions e.g. counting up one part of a word up in twos and another part of the same word down by ones. Use them and you may come up with the definitive random number generator for your machine!

LETTERS

* Computer Users Replacement Equipment *

The organisation was formed in September of last year and draws its membership from schools and colleges of further education throughout the U.K. Its aim is to acquire both computers and data preperation equipment for schools etc. so that these schools can run various Computing and Programming courses on their own on-site machines.

The organisation attempts to acquire equipment at the lowest possible cost; transport etc has been arranged by the officers up till now - in fact the officers have actually moved most of the equipment themselves.

We have been fortunate enough in placing several complete computer systems within schools and we have updated many more as well as supplying data preparation equipment.

The organisation is completely non-profit making and we have been most fortunate in being granted free advertising in many computer magazines.

P.J.Mothersole (Secretary)
CURE Charles Keene College
Painter St. Leicester

HELP

Can anyone provide any data at all on Fast Fourier Transform programs.

My math is not up to designing a processor from scratch, but given the software to operate on sampled data I can take it from there.

I offer an Intel 4K RAM free to anyone supplying sufficently detailed information.

John Hawthorne 23 Iver Lane
UXB.36428 evns. Cowley Middx
UB8 2JD

FOR SALE :

Welmec 8 level papertape reader, 30cps. Nearly new, known to be working, circuit diagram, £15 ono.

WANTED :

Friden Flexo or similar 8 level TTY device, preferably with reader/punch. Up to £20 depending on condition etc., must be functional.

R.C.Selby, 145 Bedford Lane,
Feltham, Middx. TW14 9NH

WANTED :

Does anybody have, or know where there might be, a minicomputer (working, U/S, complete or incomplete) or a core store (8 or 16 bit) for sale ?.

Any information gratefully received by Tony Scott, 78 Morley Ave, Wood Green, N.22 01-888-7841

I am developing a Video-Terminal, connected to a local computer, but also including a CPU and ALU to use it as an independent calculator with possibility of vector display.

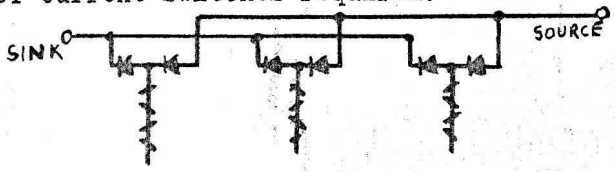
I would welcome any information at all on this kind of terminal, even at charge.

G.Depre, V.Beaudinstraat 91,
B3300 TIENEN, BELGIUM

CORE STORES

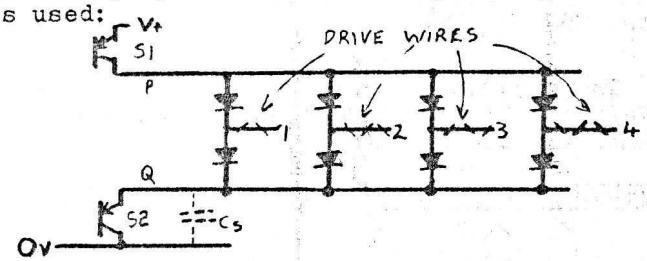
I notice that in your articles on core stores you have made no mention of the problem of stack discharge. This becomes a nuisance when the core is accessed only occasionally i.e. less than 1000 times / sec.

As you know we group the drive lines together in order to minimise the number of current switches required:

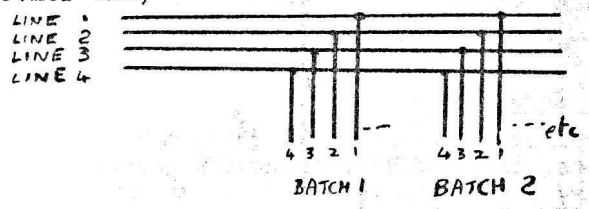


This increases the capacitive loading on the source/sink switch and I have found that if a group is left idle for a time the stray capacitances charge up to a potential which stops the current switch from working.

In my system the following arrangement is used:



When left idle point P (and therefore point Q) gradually charges towards OV. This happens to all of the batches because the lines are joined together at the other end;

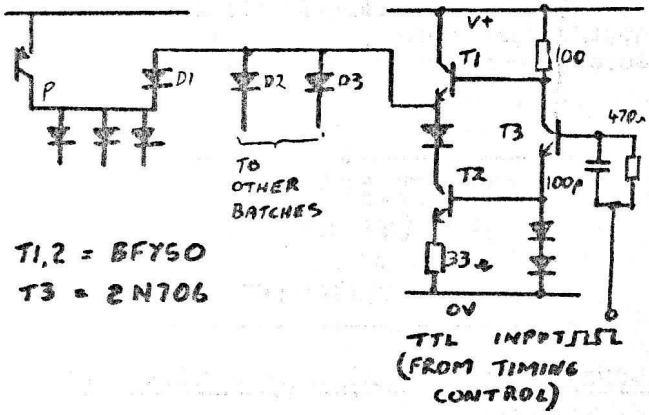


Each line being serviced by a source-sink pair.

In my case point P discharges towards ground potential and because of the heavy stray load Cs S1 cannot source current until P is at approx V+. Since it takes about 50µS for Cs to charge up S1 simply won't work.

This problem is not noticed when the core is cycled at a high rate because Cs is kept charged up. However if you try to cycle the store say once a minute it will not work.

The solution is therefore to keep P charged up to about V+, and the best way of doing this is to build a high power push-pull switch (totem pole)



During the time the core store is idle (Timing control Low) T1 clamps P to V+. When the store becomes active T1 turns off, T2 turns on reverse biasing D1, D2, D3 etc thus isolating the batches from each other and from the discharge switch (since we don't need it when the core becomes active).

T1 dissipates quite a lot of power and a clip on heat sink should be used.

LITERATURE

System 74 Designers manual, free from TI. Full of good ideas, ALU's, matrix multipliers, core sense amps and core drivers etc.

Also try & get yourself put on TI's mailing list for 'Link'. This is a quarterly bulletin of their new products but is full of interesting ideas and applications.

Anyone who is having trouble with noise on core store sense circuits should get a copy of 'The Measurement And Reduction of Noise in Co-incident Current Core Memories' by P.Cooke & D.C.Dillistane. IEE paper No 3957M, Sep 1962

J.Beard

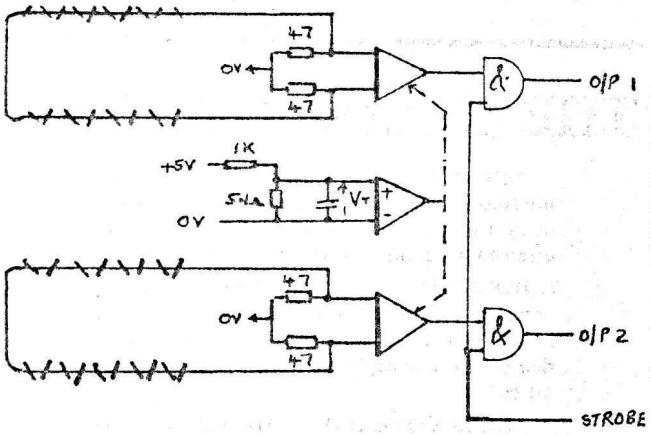
CORES FOR STORES

In the June issue of the ACCN, 711 IC's were recommended as core store sense amplifiers. It now appears that stocks of cheap 711's are running low so maybe it is time to look at a more modern type of integrated sense amplifier.

The Texas Instruments SN7524 & 7525 are dual channel sense amplifiers which detect bipolar differential input signals from the memory and provide standard TTL level outputs.

The IC in fact contains three differential amplifiers. An external reference voltage Vt is applied to one amplifier which has its output connected to the other two in such a way that it establishes an input threshold voltage for them. As the three amplifiers are all on the same chip tracking is good and the error is better than + 4mV for the 7524 and ± 7mV for the 7525.

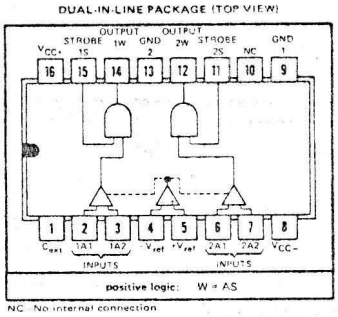
If the differential voltage applied to one of the two main amplifiers exceeds + Vt then the output will be '1' when the $\overline{\text{S}}$trobe line is '1'.



Vt (25mV in the example) is derived from a potential divider across the +5V supply. The low input current taken by the differential amplifiers allows us to use one potential divider to supply the reference voltage to a number of IC's. In practice Vt should be between 15 and 40 mV depending upon the stack output.

The outputs of the 7524/5 can drive 10 standard TTL loads each, the strobe inputs take 1 TTL load each. Current consumption is typically 25mA from +5V and 15mA from -5V

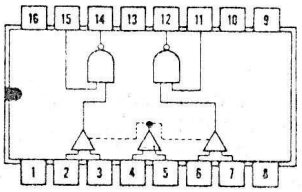
Because of the high gain, the low signal levels and the high frequency transistors used extreme care must be taken with layout (massive earth plane !) and decoupling. The two terminating resistors used for each channel should be matched to minimise the effect of common mode noise. Small low inductance capacitors should be used to decouple the supply rails and the Vt inputs as close to each package as possible. Two 'ground' pins are provided; ground 1 is internally connected to the input amplifiers and ground 2 is used by the TTL output circuits. Both ground pins should be directly connected to the earth plane which should run between the input & output pins.



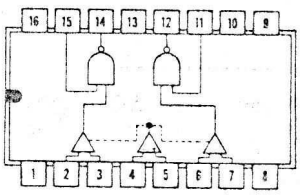
SN7524, SN7525

The SN75232 & 75233 are similar except that the output gates are inverting open collector types similar to the 7401. The 75232 has + 4mV max threshold error, the 75233 ± 7mV.

The SN75234 & 75235 are similar to the 7424 & 7425 except that NAND gates are used for the outputs.



SN75232, SN75233



SN75234, SN75235

8008 ERROR

As pointed out by some sharp eyed readers, the RETURN instruction given on page 7 of the August '74 issue of the ACCN should be;

OO ACC D11

ICL NEW RANGE

Just announced . . .
Anyone know any details ?
Let us all know please.

BOOKLIST

COMPUTER ORGANISATION & PROGRAMMING
C.W.Gear McGraw Hill 1969 390 pp

This book was written from notes for a second course in programming, it assumes knowledge of a high level language. The book discusses machine language and the design of a computer as it affects the language, then continues with an examination of software systems, programming philosophy, input/output systems, interpreters, macro assemblers and compilers.

A.R.T.H.U.R.
THE LIFE AND OPINIONS OF A DIGITAL COMPUTER

MINICOMPUTERS FOR ENGINEERS & SCIENTISTS
by G.A.Korn
McGraw-Hill

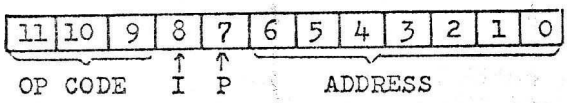
THE PDP 8

As there must be about 20,000 of these machines around now, and as the PDP-8 is the original popular minicomputer it seemed about time we did an article on it. Hopefully this article will lead in to others on such diverse subjects as control logic & assembly languages.

INSTRUCTION SET

The PDP8 uses a 12 bit word for both data and instructions. Memory is divided into FIELDS of 4096 words (the maximum number of words that can be addressed by a 12 bit binary number, each field is divided into PAGES of 128 words.

MEMORY REFERENCE INSTRUCTIONS



The seven address bits (0-6) can address any location in the page containing the instruction by making bit 7=1.

Making bit 7=0 references a location in page 0 of the current field.

Making bit 9=1 gives indirect addressing, allowing us to reference any core location in the current field by specifying (bits 0-6) the location in page 0 or the current page which holds the full 12 bit address of the operand.

Memory reference between fields is rather more complicated and is mentioned later.

OP CODE 0 : AND X ; a logical AND operation is performed between the contents of the Accumulator and the desired memory location and the result put in the Accumulator.

OP CODE 1 : TAD X ; Two's Complement Add. The Arithmetic sum of the contents of the Accumulator and the desired mem location is put in the Accumulator. The Link is complemented if there is a carry from bit 11.

OP CODE 2 : ISZ X ; Increment & Skip if ZERO. The content of memory location X is incremented by one. If the result is zero then the next instruction is skipped.

OP CODE 3 : DCA X ; Deposit & Clear Accumulator. The contents of the Accumulator are stored in memory location X then the Accumulator is cleared.

OP CODE 4 : JMS X ; Jump to Subroutine. The contents of the program counter (which is pointing to the word following the JMS instruction) is put in memory location X then the number X+1 is put in the program counter effecting a jump to X+1.

OP CODE 5 : JMP X ; Jump to X. The number X is put in the program counter effecting a jump to X.

HISTORY

Digital Equipment Corporation first introduced the PDP-8 in 1964. The original model used discrete component logic with a 1.5uS core store and a parallel arithmetic unit giving an ADD time of 3uS.

The PDP-8 was quickly followed by the PDP-8/S which was a cost reduced version using slower core (8uS) and a serial arithmetic unit (36uS ADD time) but otherwise compatible with the PDP-8. It was advertised as the first general purpose computer for under £ 10,000.

The PDP-8/I, brought out in 1968,used TTL integrated circuits and gave the same performance as the original PDP-8 but at a reduced cost and in a much smaller package.

It was followed by the PDP-8/e /f & /m which used a new architecture, provided a few new instructions and improved the performance slightly giving an ADD time of 2.6uS.The chief difference between the three models is packaging; the PDP-8/e has a larger package to accomodate more options, while the PDP-8/m is intended for building into other equipment and does not have a full control panel.

The PDP-8/A, just released, seems to be a set of boards (CPU, Memory etc.) which can be purchased separately or built into a chassis with operator panel, power supply etc. More details in a later newsletter perhaps.

Auto Indexing

When any location from 10_8 to 17_8 in page 0 of any field is addressed indirectly then the contents of that location are incremented by one before being used as the effective address of the instruction

MISCELLANEOUS INSTRUCTIONS

These have an OP CODE of 7 and are divided into 2 groups;

GROUP 1 has bit 8=0, the remaining bits having the following functions;

B7 = 1 ; CLA (Clear Accumulator)
B6 = 1 ; CLL (Clear Link)
B5 = 1 ; CMA (Complement Accumulator)
B4 = 1 ; CML (Complement Link)
B3 = 1 ; RAR (Rotate Accumulator Right). The contents of the Acc are shifted one place to the right through the link so bit 0 is shifted into the link & the previous contents of the link is shifted into bit 11 of the Acc.
B2 = 1 ; RAL (Rotate Accumulator Left). The contents of the Accumulator are shifted one bit left through the link.
B1 = 1 ; Causes the shift defined by bit 2 or bit 3 to be through two places rather than one.
B0 = 1 ; IAC (Increment Accumulator)

These commands can be combined in one instruction, for example setting both bits 6 & 7 to 1 will clear both Accumulator and link. The individual operations are carried out in the following order;

1 CLA, CLL
2 CMA, CML
3 IAC
4 RAR, RAL, RTR, RTL (RTR & RTL are 'Rotate Two places Right' and 'Rotate Two places Left')

Useful combinations include;
STL (Set Link = 1) octal code 7120
STA (Set Acc = 1 --- 1) octal code 7240
NOP (No Operation) octal code 7000

The PDP-8/e,f&m have an additional instruction ;
BSW octal 7002 : Byte Swap ; swap bits 0-6 of the Acc with bits 7-11

GROUP 2 has bit 8 = 1 and bit 0 = 0
The remaining bits have the following functions;

B7 = 1 ; CLA (Clear Accumulator)
B6 = 1 ; SMA (Skip on Minus Accumulator) Skip the nect instruction is the Accumulator contents are negative.(Two's complement arithmetic is used so this instruction tests bit 11 of the Acc which is 1 if the Acc is negative.)
B5 = 1 ; SZA (Skip on Zero Accumulator)
B4 = 1 ; SNL (Skip on Non-zero Link)
B3 = 1 reverses the skip sensing of the instruction bits 4,5 & 6.
B2 = 1 ; OSR (Or with Switch Register). The result of an inclusive OR between the contents of the Acc and the Switch Register is put in the Accumulator.
B1 = 1 ; HALT

As with Group 1 these commands can be combined in a single instruction. The individual operations are carried out in the following order;

1 either SMA or SZA or SNL (B3 = 0)
Both SPA and SNA and SZL (B3 = 1)
2 CLA
3 OSR, HALT

(SPA = Skip on Positive Acc, octal 7510
SNA = Skip on Non-zero Acc, octal 7450
SZL = Skip on Zero Link, octal 7430)

INTERRUPTS

A single interrupt line is used which when asserted by a device requesting an interrupt causes a JMS to location 0 if the interrupt circuitry has been enabled.

Two instructions control the interrupt circuits;

ION : (turn Interrupt On) enables the interrupt circuits. Octal code 6001

IOF : (turn Interrupt Off) disables the interrupt circuits. Octal code 6002

INPUT / OUTPUT INSTRUCTIONS

These have an OP CODE of 6. Bits 3-8 are used as a device selection address. Bits 0-2 control the operation of the selected device. Exact details depend upon the particular device.

BOLT-ON GOODIES

MEMORY EXTENSION

The 12 bit word only allows you to address 4096 words of memory. To go beyond this a memory extension unit can be fitted which contains a number of 3 bit registers used to hold extra address bits (to specify the field containing the instruction or data). These additional 3 bits give a maximum of 32K words. Several additional instructions allow you to load or read the contents of these registers.

EXTENDED ARITHMETIC ELEMENT

This provides a second 12 bit register (the MQ register) and a 5 bit Step Counter together with several additional instructions including fast Multiply, Divide and multiple shifts.

The PDP-8/e,f &m are equipped with the MQ register as standard and the following instructions provided for its use;

MQL octal 7421 : MQ Load ; the contents of the Acc are put into the MQ reg, then the ACC is cleared.
MQA octal 7501 : MQ into Acc ; The result of an inclusive OR between the contents of the Acc & MQ reg is put into the ACC.
SWP octal 7521 : Swap contents of Acc & MQ register.
CAM octal 7621 : Clear Acc & MQ reg.
CLA octal 7601 : Clear Acc

CONTROL PANEL

This differs slightly between models, but typically has the following features;

LAMP DISPLAY of all the major registers (Accumulator, MQ reg when fitted,PC, Memory Data & Address Buffer reg.)

12 bit Switch Register.

START key.

LOAD ADDRESS key that puts the contents of the Switch Reg into the PC.

DEPOSIT key that stores the contents of the switch reg in the store location currently addressed by the PC then increments the PC so that a subsequent operation of the DEPOSIT key will store information in the next location

EXAMINE key that reads the content of the store location addressed by the PC then increments the PC.

CONTINUE key.

STOP key.

SINGLE STEP & SINGLE INSTRUCTION switches which in conjunction with the CONTINUE key allow you to execute only one instruction (or one part of an instruction) at a time.

We still have some sets of Vol 1 of the ACC Newsletter left. 50p per set of five issues.

mike lord

THE LOGIC BEHIND IT

DON'T THROW AWAY THAT DTL

part 1 GATES

Back in 1968 or thereabouts there was a big fight going on between the manufacturers of TTL and DTL integrated circuit logic. In many ways they were very similar; a single 5V supply rail, similar input & output drive levels, same package (once everyone had adopted the DIP). True that DTL was somewhat slower but then its internal circuitry was more familiar to designers weaned on discrete component logic.

In the end of course TTL won the day but there is still a lot of DTL about and it can still be picked up for less cost than the equivalent TTL so, let's see what can be done with it.

First we shall look at the internal circuitry used for the simple gate functions. Fig 1 shows a 2 input DTL positive NAND gate while Fig 2 shows the equivalent TTL circuit.

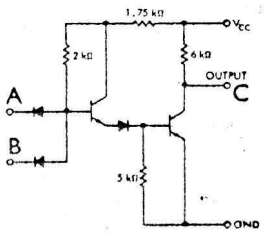


Fig 1

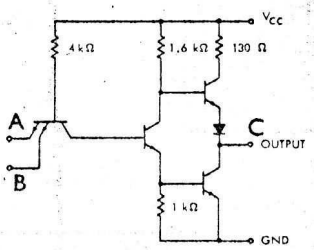


Fig 2

Not only is the logic function of the two circuits the same (A high AND B high gives C low) but the voltage and current levels are compatible;

	TTL	DTL
'0' input voltage :	0.8	0.8
'1' input voltage :	2.0	2.1
'0' input current :	1.6mA @.4V	1.5mA @0V
'1' input current :	40uA@5.25V	5uA @ 4V
'0' output voltage:	.4V @16mA	.4V @ 12mA
'1' output voltage:	2.4V @.4mA	2.5V@.12mA

Therefore; 1 standard TTL gate output can drive 10 TTL or 11 DTL gate inputs.
1 standard DTL gate output can drive 8 DTL or 3 TTL gate inputs (when driving TTL the low '1' state drive capability of DTL is the limiting factor, but more of this later)

and in practice these figures, which are based on manufacturers' 'worst case' limits can be bent a bit.

Power consumption is similar at around 10mW per gate.

DTL is somewhat slower than TTL, mainly because is uses a 6K resistor to pull the output up rather than the low impedance obtained from the TTL emitter-follower. This means that stray capacitances are charged up more quickly towards '1' by TTL .In most practical cases the DTL gate is 20 - 40 nS slower than TTL, not too much of a problem for the amateur who doesn't mind giving up that last ounce of speed. In fact the TTL output circuit causes some problems, as when the output changes from 0 to 1 or back both of the output transistors are conducting at one part of the transition, putting a lowish impedance across the supply lines which takes a short 20 - 30 mA current spike. This spike flows in the supply lines and can cause noise problems unless they are well decoupled.

The 'WIRED OR'

If you connect the outputs of 2 or more DTL gates together (Fig 3) then any condition which would make the output of an individual gate go to 0 (low) ie; A and B=1 OR C and D =1 OR E and F=1 will make the common output go to 0. This trick won't work with TTL as their outputs have a low impedance in both 0 and 1 states - so you could get a state where one gate is trying to pull the common line to '0' while another gate is trying to pull it to '1' ; a condition which might make the I/C's get a bit warm and would definately give an undefined logic level.

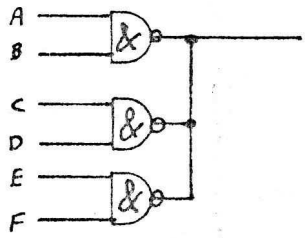
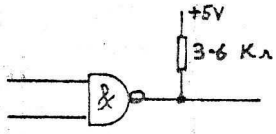


FIG 3

Of course the TTL boys have produced special 'open collector' gates like the 7401 which allow you to 'wire OR' because they don't have the top output transistor. In this case you need to add an ,external, resistor to pull the output line towards +5V, and this is the resistor which is already provided in DTL



The number of DTL gate outputs you can connect together depends upon the number of inputs driven by the common output; by doing a worst case calculation we get the following table;

Number of DTL gate o/p wired together	1	2	3	4	5	6	7	8	9	10	11
Max DTL i/p driven	8	7	7	6	5	5	4	3	3	2	1
Max TTL i/p driven	3	7	6	6	5	4	4	3	2	2	1

Note that a wired OR of 2 to 7 DTL gate outputs can actually drive more TTL inputs inputs than a single DTL gate can. This is because the additional 6K pull up resistors provide more '1' level output drive. We can therefore persuade a single DTL gate to drive more than 3 TTL inputs by adding a pull up resistor;

The increased '1' level drive, whether obtained by adding a resistor or by using the 'wired OR' function, actually reduces the propogation delay.

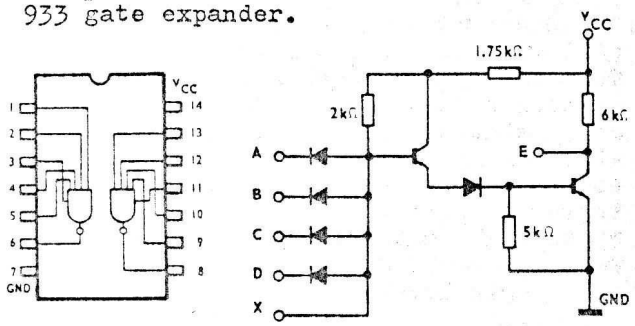
So those DTL gates are useful - as a general replacement for TTL in non-critical applications where their lower speed does not matter, and as a useful choice for 'wired OR' applications.

WHAT THEY ARE

930 Dual 4 i/p expandable gate

Fairchild or SGS DTuL9930 or U6A993059
ITT 930
TI SN15830N
Motorola MC830P or MC930P

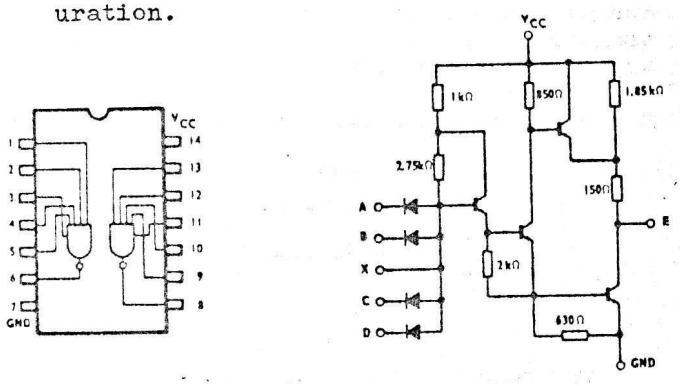
Input X is used for connection to the 933 gate expander.



932 Dual 4 i/p expandable buffer

Fairchild or SGS DTuL9932 or U6A993259
ITT 932
TI SN15832N
Motorola MC832P or MC932P

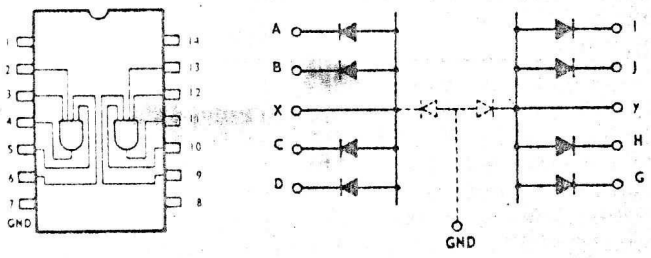
TTL type output circuit gives a '0' level output drive capability of 36 mA, '1' level output drive of 2mA therefore it can drive 22 TTL or 25 DTL gates. It cannot be used in a 'wired OR' configuration.



933 Dual 4 i/p expander

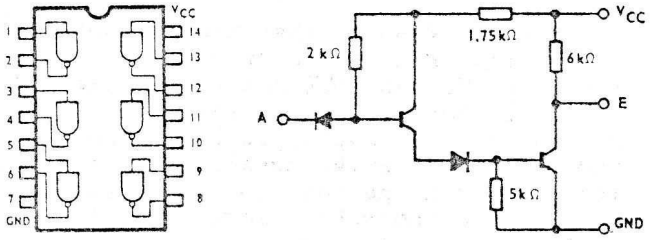
Fairchild or SGS DTuL9933 or U6A993359
ITT 933
TI SN15833N
Motorola MC833P or MC933P

For use with 930/932/944 to make n input gate.



936 Hex inverter

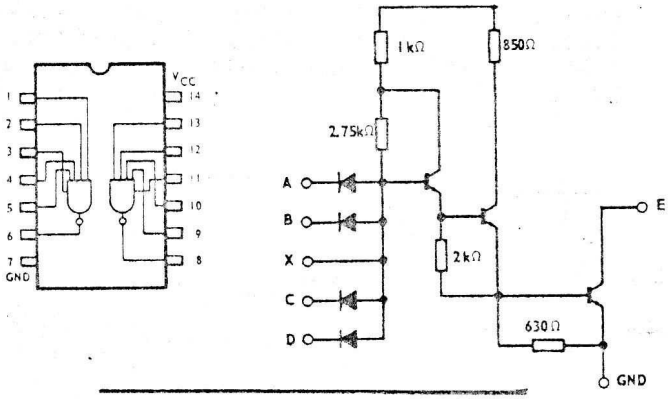
Fairchild or SGS DTuL9936 or U6A993659
ITT 936
TI SN15836N
Motorola MC836P or MC936P



944 Dual open collector 4 i/p gate

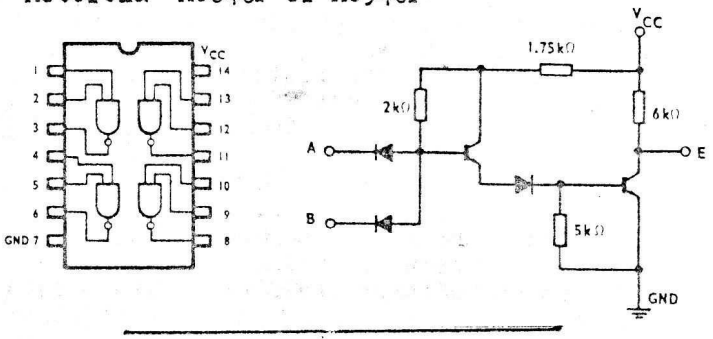
Fairchild or SGS DTuL9944 or U6A994459
ITT 944
TI SN15844N
Motorola MC844P or MC944P

Output give '0' level drive of 40mA, but don't take the output above +6V



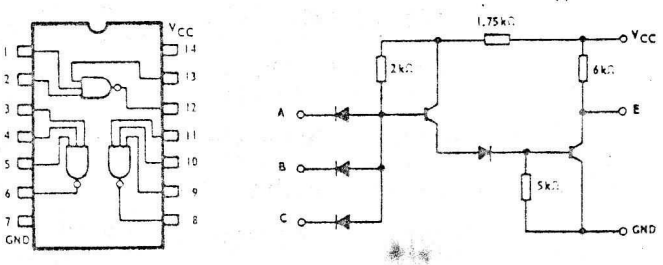
946 Quad 2 i/p gate

Fairchild or SGS DTuL9946 or U6A994659
ITT 946
TI SN15846N
Motorola MC846P or MC946P



962 Triple 3 i/p gate

Fairchild or SGS DTuL9962 or U6A996259
ITT 962
TI SN15862N
Motorola MC862P or MC962P



AMATEUR COMPUTER CLUB NEWSLETTER
Vol 2 Iss 4 October 1974
7 Dordells, Basildon, Essex

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I.Whitworth	83 Southbrooke Ave, Hartlepool, Cleveland TS25 5JB
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