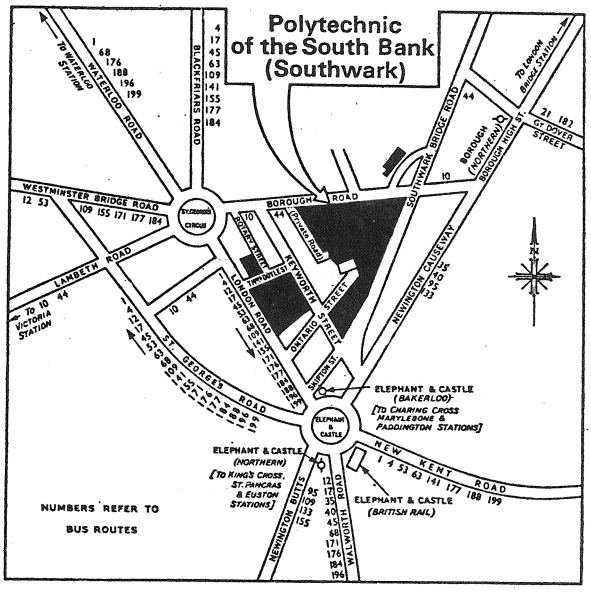
A.C.C NEWSLETTER VOL 3 ISS 6 FEB 1976



ACC ANNUAL GENERAL MEETING

Thursday April 1 7.30pm
South Bank Polytechnic

AGENDA

a) Retiring Officers' reports and statement of the club's accounts.

b) Election of officers and committee members for 1976/7.

c) Discussion of special project topics.

d) Visit and lecture programme ideas.

e) A.O.B.

Texas Instruments 9900 16 BIT MPU

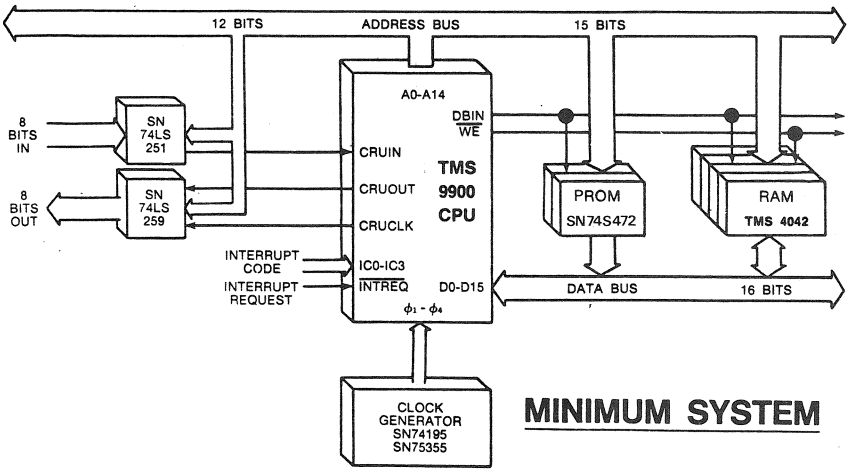
TI have now announced that this single chip 16 bit MPU will be sold separately (it is used in the recently announced 990 /4 single board microcomputer). One off price will be £59 at first (expect this to fall to about £40 by the end of the year) and small quantities will be available from April.

The device requires a four-phase 3MHz clock and +12, +5, -5V supplies.A 64 pin package is used to provide separate 16 bit data and address busses (TTL compatible). The instruction set has 69 basic instructions including 16 bit hardware multiply/divide, provides 7 addressing modes (direct register, indirect register - also with auto increment, indexed, direct main memory, immediate and program counter relative). Four shift instructions (arithmetic left & right, logical & circular) can shift any number of bits from 1 to 16.

The 9900 has been designed for very fast context switching (interrupts or subroutines) as the 16 registers used are in fact located in main memory rather than on the MPU chip, in a 'workspace' referenced by a special 'workspace' register on the MPU. The other programmer-accessible registers on the MPU are the Program Counter and the Status Register. By removing most of the registers from the MPU, and by the use of a 16 bit architecture which simplifies the on-chip control circuits, TI say that they can make the 9900 on a smaller chip than that used for their 8080 8 bit MPU !

10 of the 16 workspace registers are truly general purpose and can be used as accumulators, index reg etc. R0 can define the number of bits to be shifted in a shift operation. R12 is used in addressing I/O devices. R11 holds the previous PC after a 'branch & link' instruction, while R12,13 & 14 store the Workspace Pointer, Programme Counter & Status Register after a context switch. Context switching is achieved by storing the WP,PC & SP, then modifying the PC to point to the start of the new instruction sequence, and the WP to define a new workspace area in main memory. Thus there is no need to save the contents of the registers when an interrupt occurs.

Although the MPU chip itself is more expensive than 8 bit MPU such as the 8080, the memory saving which must result from its more powerful instruction set surely makes it attractive for the serious amateur.



MINIMUM SYSTEM

In This Issue

JIM 18

J Beard

18 bit minicomputer

'Jim 18', the peoples' processor, is now working for the revolution. Due to bad engineering design the cycle time is being kept secret.

General Features

18 bit word size
2's complement arithmetic
8 memory addressing modes
8 general purpose registers, AC0 - AC7
Interrupt system
Basic memory of 16k unreliable core store

Registers

OV 1 bit reg, set on arithmetic underflow or overflow
PC Program counter, 17 bits
MAR Memory Address Register, 17 bits
IR Instruction Register, 18 bits
SR Switch Register & Display, 18 bits. Used to display the contents of various registers on the front panel, and as a latch when loading the switches into registers. Also used as temporary storage during instruction execution.
AC's 0 to 7 8 general purpose registers, 18 bits. AC's 0 & 1 have special uses.

After an Interrupt is received, the value of the PC is loaded into AC0, and then the PC is cleared, so the next instruction executed will be at loc 0.
AC1 is used as the index register.
Also, all the unused instruction codes generate an internal interrupt (these interrupt regardless of whether the interrupt system is on or off). This gives a number of user defined instructions.

Peripherals

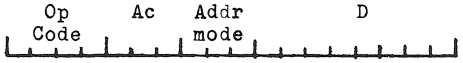
PT reader, Friden Flexowriter, 5 track punch, & a funny ¼" mag tape unit from Galdor.

Address Modes

decimal		address
0	Relative, forward	PC + D
1	Relative, back	PC - D
2	Direct, Page 0	D in page 0
3	Direct, indexed	AC1 + D
4	Relative, indirect	Pointer in PC + D
5	Relative, indirect	Pointer in PC - D
6	Page 0, indirect	Pointer in D, page 0
7	Indexed, indirect	Pointer in AC1 + D

Page 0 is the first 256 locations of memory
In indirect addressing, bit 17 of the pointer is the flag;
If B17 = 0, next address is the data
If B17 = 1, next address is another pointer

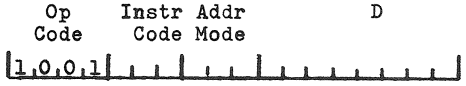
Memory Register Instructions (Op codes 0 to 8)



Op Code	Mnemonic	Description
0	ADD	AC plus addr, result to AC
1	SUB	AC minus addr, " " "
2	LDA	Load contents of addr into AC
3	STA	Store AC at addr
4	NOR	Logical $\overline{(AC + Addr)}$ to AC
5	IOR	Logical (AC + Addr) to AC
6	SWP	Swap AC and addr
7	CSE	Skip next instr if AC = addr
8	II *	unused

*Internal Interrupt

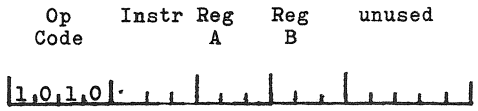
Memory Only Instructions (Op code 9)



Instr

0	CLR	sets addr = all 0's
1	SET	sets addr = all 1's
2 - 5	II	unused
6	SPC	store (PC+1) at addr
7	JMP	unconditional jump to addr + 1

Double Register Instructions (Op code 10)



Instr

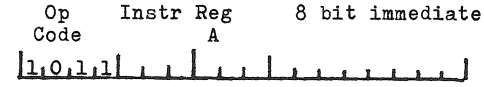
0	ADD	A plus B, result to B
1	SUB	B minus A, result to B
2	CPY	Copy A to B, B unchanged
3	NOR	Logical $\overline{A + B}$, result to B
4	IOR	Logical A + B, result to B
5	CSE	Skip next instr if A = B
6 & 7	II	

Double Register Instructions (Op code 11)

Instr

0	CLR	Sets ACB = 0
1	SET	Sets ACB = all 1's
2	TCP	2's comp of ACA to ACB
3	ISZ	Increment ACA, put result into ACB, & skip if result = 0
4	DSZ	Decrement ACA, put result into ACB, & skip if result = 0

Immediate Instructions (Op code = 11)

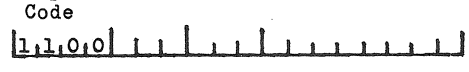


Instr

5	CSE	Skip if Reg A = Immed
6	ADI	Reg A = Reg A + Immed
7	SUI	Reg A = Reg A - Immed

Decision Instructions (Op code 12 ; relative f'wd.) (Op code 13 ; relative back)

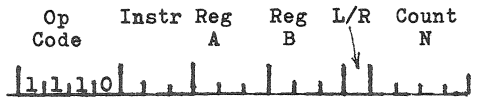
Jump Address = (PC ± D) + 1



Instr

0	JLZ	Jump if AC 0
1	JLE	Jump if AC 0
2	JEQ	Jump if AC = 0
3	JNZ	Jump if AC = 0
4	JGZ	Jump if AC 0
5	JGE	Jump if AC 0
6	JMP	Unconditional Jump
7	II	Unused

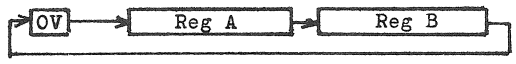
Shift Instructions (Op code 14)



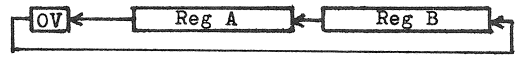
Instr

0	RTR or RTL	Rotate Reg A left/right (N+1)
1	SHR or SHL	Shift " " " " "
2	ASR or ASL	Arith shift Reg A left/right (N+1)
3	LRR or LRL	Long rotate Regs A, B L/R (N+1)
4	LSR or LSL	Long shift " " " " "
5	LAR or LAL	Long arith shift A,B " "
6 & 7		Unused

Long rotates & shifts right;

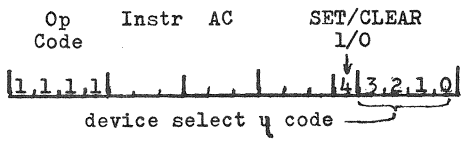


Long rotates and shifts left



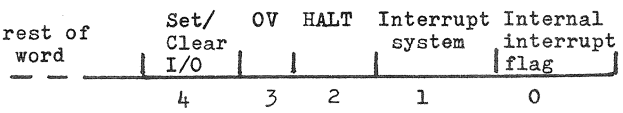
Input / Output - Machine Control Instructions (Op code 15)

Machine Flag Control & Tests



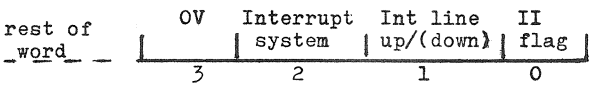
Instr

0	CTL	Set/Clear selected device



Instr

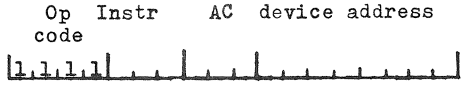
1	SKP	Skip if OV/Interrupt system/interrupt line/internal interrupt flag are set



Instr

2	SAC	Switch Reg to AC, load the first 9 switches into the AC

Input / Output



Instr

3	IPC	Transfer device status field from peripheral to AC
4	IPD	Transfer data word from peripheral to AC
5	OPC	Output control field from AC to per.
6	OPD	Output data field from AC to periph.
7	II	

* I am now making progress with my Flexowriter, however I would like to get hold of a manual for the thing, can anyone help ?

Mr J Beard 13 Mayesford Rd.,
Chadwell Heath , Romford, Essex

*

WB·2 AND BEYOND

Through the comprehensive description of its design, which links each instruction to the hardware executing it, the Weeny Bitter provides an excellent introduction to the practicalities of processor hardware, particularly for the software man and the beginner. Furthermore, because of the simplicity, it is cheap to build and any hardware problems should prove easy to debug. However, it should be realised that excellent though it is, the Weeny Bitter is a little too slow, a little too small and a little too traditional to form the heart of any computer system in which extensive development is envisaged. Also, it is based on traditional concepts and consequentally follows the general pattern of the many microprocessors currently flooding onto the market. However, these critisisms aside, the WB is proving to be a great success, being both educational and encouraging the interchange of ideas amongst members. Also it will give many people their first chance of 'hands on' usage of a computer. Perhaps for its next project the ACC with its vast pool of talent should work nearer the current boundaries of design, both from a hardware and software point of view.

Another of the major driving forces underlying the project was the design of a universal ACC processor, so that both the hardware and software could be developed throughout the club, with each member contributing his experience of a particular field. Continuing in this vien, perhaps we should try to design some machine employing the WB, so that it may be developed in a similar manner. The cassette data recording system which has been the subject of much interest and discussion recently would seem to be an obvious choice, using the WB as the heart of a microprocessor control unit. One possibility would be a small system based around key, CRT and cassette facilities. Consider the cassette as being divided into 80 byte records, so that each record may contain the same amount of data as a punched card. Thus the cassette could replace a large, bulky and expensive deck of punched cards for use as input to either the next generation ACC processor or a central ACC computer system. Data keyed is viewed on the CRT and any part may be rekeyed as necessary to correct keying errors. Once satisfied, the operator writes the record to the cassette and proceeds with the next.

The advantages of using a cassette are numerous. Firstly it is less bulky and less expensive (because of reusibility) than punched cards. Furthermore, records may be readily updated; one simply searches the cassette for the particular record (either by content or sequential record number), rekeys the data where necessary and then writes the modified record back to the cassette. Card punches provide for data entry format programs which force alpha or numeric shifts in (or the skipping of) regions of the card for ease of use. Obviously this facility should also be provided on a key to cassette machine. Another useful enhancement would be a printer attatchment, so that a hard copy of a cassette or a particular record may be obtained. This would be useful if a central ACC computer system were established; for the output could be written to a user's cassette, the user then printing down the data on his own facility. Such a system would involve a considerable amount of development, but the universal adoption of the WB as the microprocessor would allow for the modular design of the micro code, with various people writing specific areas of control. To make the maximum use of the WB the machine should be developed with the minimum use of hardware and the maximum use of micro code. Having written microcode for a similar commercial machine I would suggest that a fully featured version would require around 12k of WB2 code. If 4k - 8k of RAM were added the machine could be used

to execute the programs written on the cassette, thus providing a stand-alone system. Note that in this mode the cassette could be used as backing storage.

A major use of the 'amateur computer' is game playing, consequently the development of a sophisticated CRT display unit, based araound the WB may be of benefit to members. A VDU type machine, that is displaying a defined character set on defined lines, is a little too limited for all but the simplest of visual games. Consequently it may be useful to design a vector display unit, so that true computer graphics may be undertaken. A library of standard shapes, such as circles, squares or stars etc could be established. This is not as easy as it sounds, for each shape must be randomly lacatable and orientatable. Then of course once the problem has been solved in two dimensions we can attack three dimensional graphics. Furthermore, with suitable libraries and application programs, it could also double as a VDU. Again the machine should be developed with the minimum use of hardware and the maximum use of microcode.

Another use of the WB could be to control a mass storage system using multiple cassette drives. Perhaps for use in the implementation of virtual storage on the next generation ACC processor, as this would allow for reduced size and hence cost of main store.

Obviously, the above aim to make maximum use of the WB and the minimum use of extra hardware, as this represents additional cost and defeats the purpose of the WB project. Further, an industrial premise is that microcode and ROM is cheaper than hardware, both for maintenance and design update. This could prove to be the case for the ACC, particularly if erasable ROM were purchased in bulk and a ROM blowing service (employing a WB of course) established.

Anyone considering using a cassette may like to know that both Goldring-Lenco and Garrard market suitable chassis units, at around £20 each. These consist of a cassette transport mechanism and heads. Suitable read and write amplifier designe are published regularly in the electronics periodicals.

Mick Reeve

CALCULATOR TRIG.

TRIG ON NON-TRIG CALCULATORS

To elucidate let me explain how it could be implemented.

1) FORTRAN - angle measured in radians

```
COSINE = ANGLE/2**N
COSINE = SIN(COSINE)   this step may be completely omitted.
DO 1 I = 1 , N
1  COSINE = 2 * COSINE * COSINE
```

2) On a reverse polish logic notation calculator

Enter angle 32 ÷ x + 1 - x + 1 - x + 1 - x + 1 - x + 1 -

Note that N = 5 so $2^N = 32$ for this example.

Actually a more efficient way to arrive at the same result is;

Enter angle 16 ÷ x 2 - x 2 - x 2 - x 2 - x 2 - 2 ÷

3) On a calculator with algebraic logic

Enter angle ÷ 32 x = + = - 1 x = + = - 1 x = + = - 1 x = + = - 1 =

4) Example ;

Suppose one has a calculator which only calculates trig functions from 0 to 90^0 and one wishes to calculate the COS of 359^0.

Entry	Display	Comments
359	359.	Enter angle
+4=	89.75	Divide angle by suitable power of 2
sin	0.99999	The COS function could be used instead
x=	0.99998	square
+=	1.99996	double
-1=	0.99996	subtract 1
x=	0.99992	square
+=	1.99984	double
-1=	0.99984	subtract 1 gives result
1 COS	0.99984	check result by looking at COS of 1

in this example N=2, so $2^N = 4$

5) to find COS 30^0 on a non-trig algebraic calc.

30 ÷	30.	Enter angle
57.295	0.5236058	convert to radians
÷ 16	0.0327253	divide by power of 2
x=+=-1x	-0.9978581	square, double, subtract 1
=+=-1x	0.9914416	" " "
=+=-1x	0.9659128	" " "
=+=-1x	0.9318256	" " "
=+=-1x	0.865975	"""gives result
=	0.7499127	$\cos^2 30^0$ should be 0.7500000

In this example N=4 so $2^N = 16$

It has been assumed that sin 0.0327253 = 0.0327253

To Calculate Cosine or Hyperbolic Cosine

step 1) Divide X by a power of 2 say 2^N where N must be a positive integer

step 2) Either; take cos of result
or; take sin of result } for COS
or; take cosh of result for cosh

step 3) Must be carried out N times
a) Square previous result
b) double previous result
c) subtract 1 from previous result

result is cos or cosh X depanding on step 2

Notes;

N should be chosen such that step 2 is sufficiently accurate. For small X ;

(X must be in rad) $\sin(X) = X$, $\cos(X) = 1-X^2/2$, $\cosh(X) = 1+X^2/2$

Thus by omitting step 2 altogether, implying an approximation to sin, trig can be implemented on non trig calculators.

The algorithm is based on the facts that;

$\cos(2X) = 2.\cos(X).\cos(X)-1$
$= -(2.\sin(X).\sin(X)-1)$

$\cosh(2X) = 2.\cosh(X).\cosh(X)-1$

Bill

LOCAL GROUPS

Mr D Monro would like to hear from anyone who would be interested in forming a local ACC group in the Ipswich / Colchester area.
7 Anderson's Way, Woodbridge, Suffolk IP12 4EB
tel; Woodbridge (039 43) 3267

●●●●●●●●●●●●●●●●●●●●

Cambridge Computer Constructors - we're a very informal group of students who are pooling money and information to construct a machine. Plans at present are for an 8080 based processor so that we can get something working fairly quickly. If this goes OK then a more sophisticated 24 bit number cruncher has been suggested. Anyone interested please contact me.
Bob Whitaker S19 Whewell's Court
Trinity College Cambridge CB2 1TQ

LETTERS

HITS & FRENCH DATES

I received yesterday the December issue of the ACC newsletter. So, you have reached the same opinion as I did about HITS. This is confirmed by Prof.J.D. Nicoud who wrote me after publication of this proposal in the bulletin de l'AFACO :

"Nous avons experimente et abandonne les schema et programme proposes par POPULAR ELECTRONICS.."

The main purpose of this letter is to comment the item "computer dating" by R.Baker. In the item "calendrier" in Encyclopedia Universalis III, 793 Dr Andre Boischot from Meudon University wrote; ".. en 1582.., a Rome, le vendredi 15 Octobre succeda au jeudi 4 Octobre .."

I enclose the algorithms published: first, many years ago by B Clark and Peter Stumpff at the National Radio Astronomy Observatory (USA); second recently, by M Dreyfus and C Gangloff in "la pratique du Fortran" (Dunod, 1975 p 168) ** see below ed***

M Dreyfus

EEC DATES

I'm afraid that Mr Baker ("Computer Dating") has oversimplified the pre-1752 algorithm. I wonder if he has tried taking a random 'Lord's Day' from Samuel Pepy's diary - the algorithm comes out with Monday !

The error is that the event of 1752 was not simply a correction of 11 days, but the changeover from the Julian to the Gregorian calendar. The rule that the century years are only leap years if divisible by 400 applies only to the Gregorian calendar. Mr Baker's 'Table A' relies on the fact that events repeat themselves every 400 years. Before 1752 the corresponding period is 700 years, so that we divide the century digits by 7, and Table A, column 1, becomes;

Rem	Working Figure
0	4
1	3
2	2
3	1
4	0
5	6
6	5

and all century years are leap years when looking up Jan & Feb in Table B.

We also have to be a bit more careful with years BC. There was, of course, no year zero. This means that to get an equivalent year we have to add 701 to a negative year, so that 10BC becomes 701 + (-10) =691. Of course, the Julian calendar itself only began on Jan 1 45BC, so that it does not make sense to apply the algorithm earlier than that.

At the risk of adding further confusion, it should be pointed out that the 1752 changeover does not apply everywhere. When Pope Gregory XIII introduced the New Style calendar, the error was 10 days, and October 15 1582 followed October 4 1582 in Italy, France, Spain and Portugal. I believe that Scotland changed over in 1600.

I hope that this has clarified things.

Finally, a quick word about the newsletter. Looking through back issues I see that it has improved quite a lot since it started. May I suggest that a plea be made for software published in the newsletter or otherwise made available to members to be a little more machine independent ? In particular, I would like too see a transportable WB simulator, (written in something like BCPL, which will run on just about anything). I might write this myself if I get time - if I do I will let you know.

Martyn Johnson

SLICES

Perhaps members would be interested in two products I am currently working with, although they are probably well outside the amateur' price range. These are the Advanced Memory Devices AMD2901 and the Monolithic Memories MM6701. Both are very similar, only speed and price differences, although they are not direct replacements for one another. The devices are 4 bit slices containing 16 registers, an extension register, and a complex Arithmetic /logic /shift capability. Cycle times are between 200 - 300nS (AMD faster) and with the addidtion of a ROM microprogram can compete with the speed & capabilities of many minicomputers. The price is about £30 each (one off) but this has dropped from £100 a year age and the competition between the two is forcing it lower. Even so £120 for a 16 bit machine plus microprogram ROM puts this out of the range of many pockets.

S W Burr

SHOP

FOR SALE

1 8k x 18 Mullard Core (type AW3805), cased, with connections to stack via 20 Amphenol sockets. Complete with manufacturer's data etc. £25

20 sheets 8.3" x 8.4 " double sided fully pierced Veroboard 0.1" matrix. Vero part No 1260 £25 or £1.50 per sheet.

1 Vero Card Frame, type 3C/4UC1/D2w1/MR4/L2G2/.5 New and in manufacturer's packing £10

16 SN74181 and 5 SN74182 £30 or '181's at £2 each.

M Reeve 6 Limes Ave, North Finchley, London N12 8QN

Has anyone got a manual for the GI 1600 MPU I could borrow for a few days, will refund postage.
mike lord

Clark & Stumpff's algorithm

```
      REAL FUNCTION DJL*8(IY,IM,ID)
C     NRAO 5/1 F(D) DJL F4S LCD=5
      JDN=(IM*3057)/100+ID+((5-IM/3)/5)*(2-(4-MOD(IY,4))/4+
     1   (100-MOD(IY,100))/100-(400-MOD(IY,400))/400)+1721028
     2   +(IY*365+IY/4-IY/100+IY/400)
      DJL=DFLOAT(JDN)-0.5D0
      RETURN
      END
```

Dreyfus & Gangloff's algorithm

```
C DATE DU CALENDRIER JULIEN EN FONCTION DE LA DATE DU CALENDRIER GREGORIEN
      INTEGER FUNCTION DATE2 (I, J, K)
      DATE2 = K-32075+1461*(I+4800+(J-14)/12)/4+367*(J-2-(J-14)/12*12)/
     1        12-3*((I+4900+(J-14)/12)/100)/4
      RETURN
      END
```

.... SHOP

FOR SALE

Ex-BEA VDU as received from Chiltmead £30 ono
J Green 01 573 3888 ext 2901 (day)
48 Princes Park Lane, Hayes, Middx

CDC 9450 DISC STORE
Self contained, housing a number of sub-units i.e. acuator,motor drive, power supply, read/write logic. The logic circuitry is built on a large number of plug-in boards. All input/output lines are terminated via two multi way connectors. The unit requires a power input of 220/440V three phase, however with a few minor alterations, everything except the drive motor will operate from a single phase 220V supply. The drive motor is a 1/3 HP 3ph motor, which would require replacing with a similar single phase type.

Apart from the one complete unit, I have thousands of spare parts. The only thing I can't supply are disc packs. To my knowledge the equipment is complete, but it will be sold untested. These units are currently advertised in 'Wireless World' at 'from £450'. Best offer around £50 secures.

Total capacity 8,192,000 6 bit characters.
819,200 char / disc surface, 4096 / track.
Max access time 165mS
One track access time 25 - 27 mS
Double frequency recording, 756 BPI (outer track)
Data transfer rate 208,333 characters / sec.
Disk packs; 6 discs, 10 usable surfaces.
200 tracks / surface + 3 spare
14" diameter. 2400 ± 48 rpm
Heads; 10 total.
Overall dimensions; 40¾" high, 36" deep, 24" wide
480 lb weight.

D.J.Barrow 47 Cannon Lane, Stopsley, Luton, Beds

WANTED

Algol 60 compiler manual suitable for an ICL 1900 series computer, also a 'bindump' of the PL/1 compiler on tape or the conversion of PLAN to machine code !!! We have been given a new BASIC compiler JBAS Mark 2 it includes alphanumerics and TAB functions; has anyone got a compiler manual ? We would like to establish terminal contact with another terminal i.e. 'back to back' with someone in the London area . The address of my school is;
Purley High School for Boys, Placehouse Lane,
Old Coulsden, Surrey CR3 1YA
or they can be directed to my home address ;
46 Manor Wood Road, Purley, Surrey CR2 4LE

G A Tompsett

WANTED

5 channel paper tape punch & paper tape.
R W Davey 'Woodbine Cottage', Church Lane,
Saltfleetby-all-Saint, Nr Louth, Lincs
tel Saltfleetby 642

TTY 28

I have the parts manual and technical manual for the Teletype 28 send/receive terminal, which I would be prepared to lend to members (at their expense as regards postage).
C.D.Ward 3 Northway, Morder, Surrey. SM4 4HE

ALGOL 8080

I am currently writing an algol simulator for the Intel 8080. If any ACC mambers are interested would they please write to me (a SAE would be helpful)
Bruce Haxton ATE III , B watch tels, LATCC,
Porter Way, West Drayton, Middlesex.

WB

I am enjoying the ACC newsletter, particularly the Weeny-Bitter. I have been converting A Fisher's simulator program to run on our 1905E. It would be interesting to hear what, if any, software has been written for it. I will be writing some routines first, character handling routines and arithmetic functions. Somebody may have already done this though.

I am trying to pluck up courage to build a WB. I would consider myself a fairly experienced constructor, I am a radio amateur, and have built a transmitter, an oscilloscope and several radio receivers. But I am intimidated by the number of connections between the IC pins ! It seems to me to be too easy to forget one, or make a mistake, which would be difficult to find afterwards.

Perhaps one of the constructors would write an 'informal' article on the actual construction, giving any methodical approach he might have used in doing the wiring, pointing out any snags which arose in practice. There must be other people nervous of tackling a project of this size who would find this a help, the next best thing to seeing a completed machine.

The idea of an I/O peripheral based on 7 segment indicators is a good one, since there must be many people for whom personal circumstances prohibit having a large, noisy, teletype as a peripheral. A keyboard using a TV as the VDU screen would be ideal, but is probably a year or two into the future as far as cheap, fairly simple circuits are concerned. Perhaps ACC could publish such a circuit as a follow-up to the Weeny Bitter.

It seems to me that it would be rather painful with the basic WB-1, entering programs on the switch register all the time. I suppose a modified cassette tape would be the simplest and cheapest input/output medium for such a basic machine, but I think at least a paper tape reader (a hand propelled one ?) would be necessary so that one could at least prepare ones basic programs on sombody else's terminal. Does anyone have any ideas ?

J.V.Moss Ghmizedale College, University of Lancaster
Bailrigg, Lancaster LA1 4YU

HELP

I have recently acquired an AMPEX TM7 7 track tape transport and I would be interested to hear from anyone with any experience of interfacing microprocessors or minicomputers to this or a similar device. I have a copy of the manual if anybody requires information on the transport.

I would also be interested to hear from anybody with any experience of the Intersil 6100 microproc as I am thinking of buying one of these in the not too distant future.

J Green 48 Princes Park Lane, Hayes, Middx

CHEAP IC

A short note to tell you that Electronics Today International magazine is repeating the fabulous cheap TTL/CMOS offer, which first occured in June 1975. I hope our ACCN readers can get their April ETI's as soon as they are issued, usually the beginning of March.

Steve Thompson

MPU

I went to see GIM (57 Mortimer St, W1N 7TD) and got some info on their CP 1600 MPU . 87 instructions, 8 general purpose 16 bit registers. Requires +12, +5, -3 volts supply and 5MHz 2 phase clock.

Texas' TMS 9900 MPU uses a 4 phase 3 MHz clock and needs +12, +5, -5 volts. Its 16 general purpose regiaters are defined to be contiguous memory locations, and there are 8 addressing modes. External instruction capability. Some 67 basic instrustions including multiply and divide. 64 pin.

Bill Collis

CONSTITUTION OF THE ACC

as revised and agreed at the AGM of 21/3/1974

1) The Club shall be known as the Amateur Computer Club.

2) The aims of the Club are to promote and co-ordinate interest in the design, construction or programming of computers and allied equipment.

3) Membership of the Club shall be open to anyone subject to;
   a) The approval of the ACC committee, who have the right to reject any application for membership.
   b) Payment of the annual membership fee.

4) The membership fee shall be £1 per annum except for members who are resident in the UK and who are also 16 years of age or under on the 1st. April, in which case a reduced fee of 50p shall be allowed.

5) The membership fee shall only be changed by resolution at a general meeting.

6) Membership shall last from April 1st until March 31 of the following year.

7) The committee of the Club shall consist of not more than 5 officers and not more than 10 other committee members, all of which are honorary appointments.

8) Any member of the ACC is eligible for election to the committee, provided that he or she is proposed and seconded by two other ACC members.

9) Officers of the committee must be 18 years of age or older.

10) Elections for officers and committee members shall be held at the AGM.

11) The activities of the Club shall be coordinated by the committee in accordance with the constitution.

12) All resolutions shall be carried by a simple majority of those present and voting. In the case of a tie the chairman has the casting vote.

13) All general meetings shall be held within 10 miles of the centre of London.

14) Notice for any general meeting shall be sent to members of the Club not later than 2 weeks before the date of the meeting.

15) An extra-ordinary general meeting may be called by 10 members provided that they give 6 weeks notice to the chairman and pay any costs incurred in informing all club members of the proposed meeting, and also the costs of the meeting.

16) At any general meeting a quorum shall consist of 10 members, including 3 members of the committee, at least one of who shall be an officer.

17) A resolution for the dissolution of the Club shall require a three quarters majority as a result of a postal ballot of all current members. Any assets of the Club remaining on dissolution shall be distributed among the current members, pro-rata according to their subscription for that year.

18) The address for all communications to the Club shall be 7 Dordells, Basildon, Essex.

19) A resolution to change this constitution shall only be approved at a general meeting.

M. Whelan has sent a copy of an article which appeared in the QST magazine, showing a circuit to produce a single line alphanumeric display on a TV from ASCII coded input (40 characters). Similar to the 'Telewriter' article but simpler in having only one line & no editing facilities. 4 pages. Send me a stamp if you want to borrow it.

m.lord

ED'S BIT

We've been rather overwhelmed by a sudden increase in membership as a result of the WB publicity - we now have over 400 members. This is of course just what the club needs, only drawback being that we had to get a lot of back issues reprinted (which is expensive) as previous printings had been for only 300 members. Anyway, welcome to all the new members.

As a result of this, we now have back copies of all volumes of the ACCN - see the attached membership form, which I hope everyone is going to return !

You will see that we are going into yet another year without any increase in membership subscription, this is entirely due to the increased membership. By the way, to save postage costs, 1976/7 membership applications will not be acknowledged until the April (Vol 4, Iss 1) newsletter is sent out.

I'm in something of a quandary about the WB. It has generated a lot of interest, and been generally well received, but I'm not sure whether we should proceed to the WB-2. The problem is that it would cost about £20 and take 40 - 50 IC to enhance the address and control circuits to the full capability WB-2, and for that money one can almost buy a MPU chip with the same power (although not the same elegance !), and of course far fewer connections. Could I have your opinions on this please.

You heard that the Science Museum opened its new Mathematics & Computing gallery? Well, so the story goes, one of the exhibits is a CRT terminal linked to some clever programs that the public can play with. The software was designed to be as fool-proof as possible; for instance if a user just inputs rubbish, the system waits patiently for a time, then politely asks the user to stop it. The designers were also worried by the thought of some naughty member of the public delighting in typing in naughty words for the pleasure of seeing them displayed by the computer, so they set up a file containing all such words, including variants & mis-spellings, so the computer could do a quiet bit of editing. Well, they turned the system on one morning and were pleased by the attention it was getting until they noticed that the system was printing out the entire content of the rude word file - and who said computers weren't educational ?

Regarding the ACC constructional project for next year - this will be settled at the AGM, but from the voluminous correspondence I've had (most of which I haven't been able to print through lack of space in this issue) it will probably be a VDU to work with a TV screen, possibly interfaced to a MPU to do the editing functions.

J.Creutzberg will have a WB simulator working on his DEC 10 system at the AGM, and I hope to bring my version of the WB , although I'm not sure that it would survive the journey ! So, see you there.

Finally, I've bought some 'surplus' calculator keyboards (type C) from Greenweld (see W W), and am making three of them into a full upper/lower case ASCII coded keyboard. Details in a forthcoming issue(if it works)

MPU NEWS

TI and Intel are expected to be bringing out 16k dynamic read/write memory IC this year.

•

Intel 8080A & Motorola 6800 MPU now about £28 each 1 off without VAT.
Signetics 2650 is £40.
SC/MP will be introduced in a couple of months - rumour has the one-off price as £12.50 !

•

Yet another kit from Intel; kit SDK, £191, has an 8080A MPU with 8228 system controller & 8224 clock generator, serial IO using the 8251 USART, 24 other IO lines, 256 bytes or read/write memory, and 2k bytes of PROM, 1k of which are already programmed with the system monitor, which allows the operator to communicate with the system using a TTY terminal.

•

THE WEENY-BITTER

As predicted by the cynics amongst us (i.e. those with some engineering experience),some changes are needed to the WB description given to date.

The big drop-off was in the MOV instruction - instead of moving a to b , it moved b to b, not a very useful result. Part of the problem was in the coding of the AU control inputs CA-CD (Iss 4, p 11 &12). The table on p 12 should be corrected in its eighth line to;

CA	CB	CC	CD	operation	SR	S3	S2	S1	S0	M	Cn
1	1	1	0	B	0	1	0	1	0	1	1

Then the control decoding gate array (p 11) is changed to that shown in fig 1.

Next, the gates in the control unit which drive the CA-CD lines (Iss 5 p 8) should be changed as shown in fig 2.

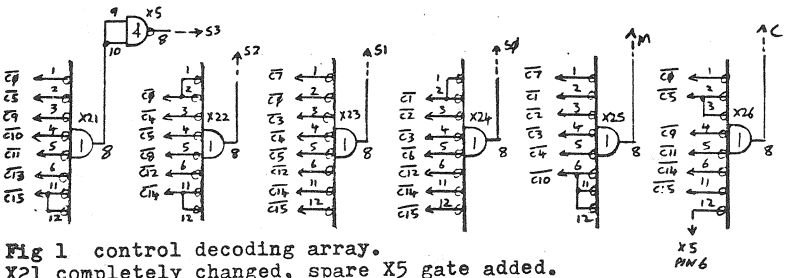


Fig 1 control decoding array.
X21 completely changed, spare X5 gate added.
Changes to X23 pin 1, X25 pin 1, X26 pin 3.

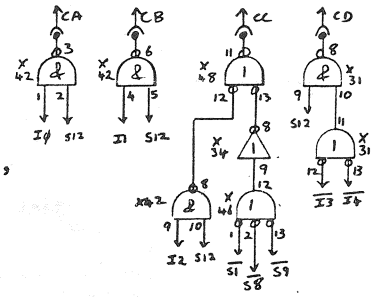
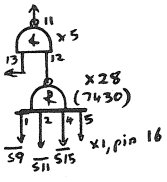
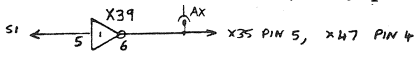


Fig 2 replaces circuit block at top left of page 8, Iss 5

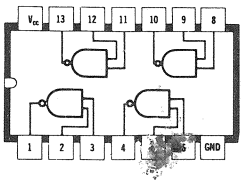
Also, it has been found that under some circumstances, the TST, CLA & SHR instructions set the C bit erroneously. To cure this an extra 4 input gate (X28) must be added as shown on the right, replacing the inverter which fed into X5 pin 12 (Iss 4 p 11).



A spare inverter from X39 should be connected so as to hold the AX line low during S1, otherwise the switch reg or the PC contents may be gated onto the data bus while we are trying to examine the content of the A register; (Iss 5 p 8)



Finally, a few minor corrections to the control unit schematic (Iss 5 p 8);
X29 pin 4 should go to I2, not $\overline{I2}$
X45 pin 2 should go to I0, not $\overline{I0}$
X45 pin 5 should go to I2, not I2



SN7401N
Quadruple 2-input NAND gate with open collector output *

Further, the pin layout given on p 14 of Iss 4 was incorrect - correct version is on left.

TESTING IT

This is really quite easy, provided that one adopts a deliberate, logical approach. The first step is to make sure that the Arithmetic Unit and Address Unit circuits work on their own, without connection to the control unit, by temporarily connecting data & control inputs to 0V or +5V as required, and checking the states of the various outputs(a 5V voltmeter is OK for this, remembering that a logic low level should be less than 0.4V, and a logic high greater than 2.4 (typically 3.3), anything inbetween is highly suspect and usually results from a gate input with nothing driving it, or, sometimes, from an incorrect connection between two gate outputs(one trying to pull high, the other striving to go low).

Next, check the operation of the memory in a similar manner, making sure that at least the first 8 locations (addresses 00000000 to 00001000) are OK.

The control unit is best checked by reconnecting it so that you can use the GO button to step through individual states (Iss 5 p 6), then check its operation against the flow chart (Iss 5 p 6), applying a dummy instruction byte to the data bus (by connecting the DATA lines to 0V for a '1', leaving them open for a '0')for state 3 (in which the instruction is latched into the instruction register.

Only when you are as sure as possible that the individual units are working should you reconnect the GO button circuit and try the complete machine.

First, make sure that you can DEPosit and EXamine, i.e. load data from the switch register into store and then display it (see Iss 5 p 5), and check all 256 locations of the store. Two things to beware ; locations 001 & 002 are the switch register and program counter, so you can't sensibly store data in them, and, after you have depressed the GO button to do a DEP or EX, the address display is showing the next address.

Finally, try some simple programs;

loc.	content			
010	030	START:	GTO START	;for ever !
011	010			

loc	content			
010	100	START:	CLA	;clear Accumulator
011	101	LOOP :	INC A	;could be INV or DEC
012	104		TST A	
013	000		HLT	
014	030		GTO LOOP	;and again
015	011			

this last program should result in 00 000 001 on the data display the first time GO is pressed, then each subsequent operation of the GO button will increment the display (or INVert it, or DECrement) Note the TST used to put the latest version of the Acc. into the A reg ready to display it when the HLT instruction is reached.

A word of encouragement; there were about 20 faults (wrong or missing connections, short circuits dry circuits & one dud IC) on my beast, but, once I'd sorted out the basic design errors, the constructional faults were found & corrected in a couple of evenings. Once you've got the machine more or less working, it is amazing how easy it is to devise simple programs on the lines of those above to test the operation of the entire machine & pinpoint any funnies, provided that a logical approach is taken at all times.

AMATEUR COMPUTER CLUB NEWSLETTER
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m.lord
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