ACC AMATEUR COMPUTER CLUB NEWSLETTER
VOL.4 ISS 4 OCT 1976

KIM-1

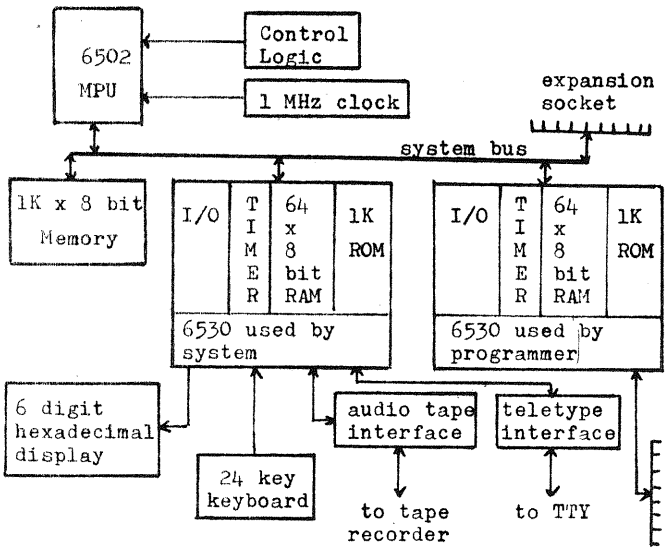
A much belated letter about my computing activities. I had intended to regale you a couple of months ago regarding proposals for a system based on the 6800 MPU chip. Luckily I 'discovered' the existance of a chip in the States which I now reckon to be superior for the amateur enthusiast. You made a passing reference to it a while back in your CPU survey newsletter but that's the only mention of it I've seen anywhere in an English magazine.

The 6800 manuals are designed for industry ; I gave up on them after a few hours ! (anyone like to buy them ?) The MOS Technology 650X series of chips are superbly and clearly documented. The 6502 in particular is Ideal for the home constructor.

Of real interest is the KIM-1 module, which I've now got fully operational. A ready-built microcomputer with tape, paper-tape and teletype interfaces, keyboard and hex display in-built. Add a power supply and away you go !. It is not known in England at all, which is a real shame. It really is good.

Future developments for me will be more memory and a VDU. When the funds run to it that is !. The only complaint about KIM is that it's only available from the States (about 4 weeks delivery) at $245 + $20 carriage + 8.4% duty + 8% VAT, total about £175. Still not bad I suppose when you realise what it is. I reckon a comparable 6800 system would be about the same.

Dennis Holman
4 Larchfields, Saughall, Chester CH1 6BU



Power; 5V @ 1.2A
12V @ 0.1A

The 'system' consists of;

1) KIM-1 Module on a printed circuit board with edge connectors and sockets.
2) 2K bytes of software; monitor programs to run the interface circuits and enable programs to be written and run.
3) KIM-1 User Manual, System Schematic.
4) 6500 Hardware Manual, Software Manual.

It is a self-contained microcomputer capable, in its basic form, of;

1) Inputting a program to its 1K of memory via its 24 key keyboard, and displaying results or memory locations and contents on its 6 digit hex display.
2) Interfacing to a standard teletype and punching or accepting programs from a paper tape reader/punch if fitted.
3) Interfacing to any domestic tape recorder;reel to reel or cassette, for bulk storage of programs.
4) Single-stepping through a program for checking and dubugging.
5) Generating fixed or variable time delays under program control by use of an interval timer on a 6530 chip.

Expansion; it is capable of expansion as follows;

1) 15 Input/Output pins are provided to run application circuits or peripherals.
2) KIM-1 contains sufficient decoding for immediate expansion to 4K of memory. With decoding chips KIM-1 can run 65K of memory.
3) External keyboards can be added directly.

KIM-1 is complete (except for the power supply). Full details are given in the User Manual (140 pages), Hardware Manual (160 pages) and Programming Manual (240 pages). Further details from MOS Technology Inc.
Valley Forge Corporate Centre
950 Rittenhouse Rd.,Norristown,PA.19401 USA

6502 MPU Chip

The 6502 is an 8 bit microprocessor with a powerful instruction set (56 commands), 13 addressing modes (including Absolute Indexed, Indexed Indirect, and Indirect Indexed), multiple interrupts, and a full 16 bit (65K) address range.

The Programming Model is of an 8 bit accumulator, Two Index Registers (X & Y, each 8 bit), a 16 bit Program Counter, a 8 bit Stack Pointer, and a 8 bit Processor Status Register (containing flags for Negative, Overflow, Interrupts, Zero, Carry, and one for setting Binary or Decimal Mode).

6530 Memory & I/O Chip

This is a composite chip containing;

1) 1K x 8 bit Read Only Memory
2) 64 x 8 bit RAM
3) A 1 to 262,144 clock-period Timer enabling timing operations or delays to be made under program control.
4) Two 8 bit input/output interfaces.

IN THIS ISSUE

ACC MEETS GIM

Peter Rush, of General Instrument Microelectronics, will give a talk on the LP8000 and CP1600 MPU and supporting chips on Thursday 25 November at 7.00 pm in room 468 at the South Bank Polytechnic ,Borough Road, Elephant & Castle.

CT also ZNA193E

CCIR/EIA
TV SYNCHRONISING
PULSE GENERATOR

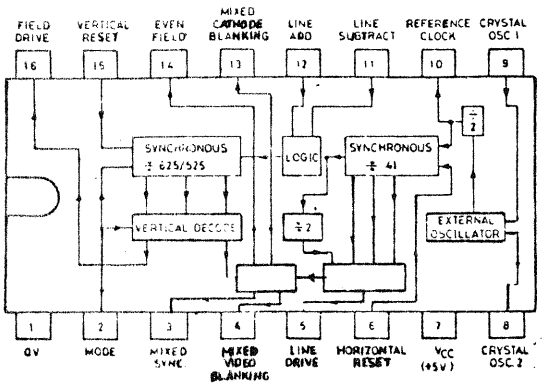
FERRANTI ZNA 134

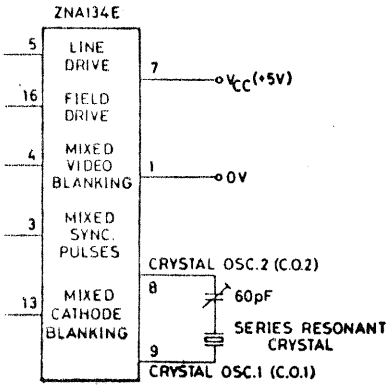
A Single Chip TV SPG

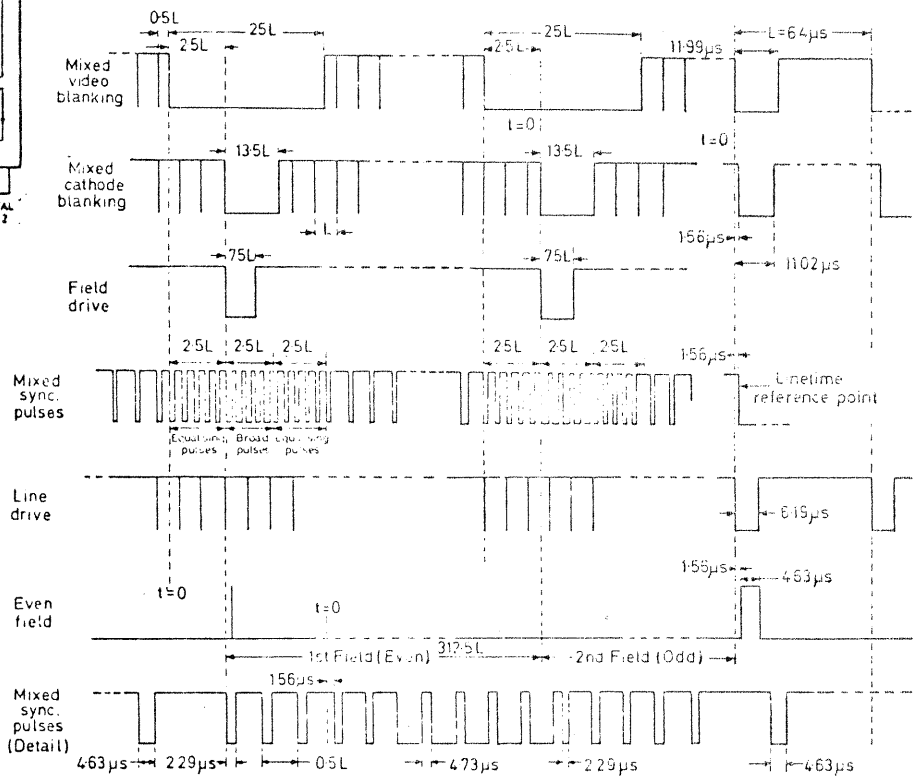
R W Warre

One of the obvious design problems that must be overcome when building a television VDU is that of providing sync, blanking and drive pulses for the time bases and display. Normally this is achieved by using TTL counters (see Elektor 18, for intance), and quite an amount of PCB space and 5V power is required to produce the appropriate waveforms. Ferranti, however, have produced a single chip TV spg, usable on either 525 or 625 line systems. Details are shown below. It can be seen that it is a monochrome device, a limitation of no consequence in VDU design. A clock oscillator of twice the required spg clock frequency can be used to generate the dot matrix characters and also, via a divider, the spg clock drive.

At present the one off price is £21 but no doubt eventually this will drop to a level where it will be a serious alternative to 'roll your own' spgs.







The ZNA 134 integrated circuit utilises a 2.5MHz* crystal to generate all the horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in 625 or 525 line commercial, industrial or military television systems. The synchronous dividers and decoding logic employed within the unit ensure perfect interlace, together with spike-free output waveforms having precisely defined relative positions and pulse widths.

*Dependent on line system used, series resonant.

OUTPUT WAVEFORMS

625 line CCIR standard output (Mode 1).

Crystal frequency = 2.5625 MHz.

Line frequency = 15.625 kHz, Field frequency = 50 Hz.

Line period = 64 µS, Field period = 20 mS.

JON'S SALE

The following letter was received from Jon Aslett in the middle of July and circulated via CHIC ; but is being reproduced here both for general interest and because Jon mentions that he is going to dispose of some more equipment early next year. He is moving at the moment but may be contacted via;
2 Park St.,Nettleton Hill,Golcar,Huddersfield.

I am now about to rationalise my computer equipment. In order to allow me to accomodate the systems I have on order (that in general are a bit too big for ACC members) I am releasing 4 of my smaller systems .

All the prices represent 60% of the cost value to me and are well under any commercial value for the equipment.

I have obtained an ICL 4/70 384 kB with 2 1350 LPM 132 pp printers, 2 900 CPM card readers, one 100 CPM punch, 1 1000 CPS paper tape reader and 110 CPS punch, 5 EDS 8 (8MB) disc drives, 6 60kC tapes 800/1600 bpi and logging printers, typewriter etc. Machine runs under 3D (soon to be 3H). This machine has 10 hardware partitions and is frightening in speed & size !

I have also contracted for a 4/72 512 kB in November.

The rest of the 'New' equipment is a Honywell H2200 and H1250 each 114 kB. 3 18MB discs, four 30/60 kC tapes on H2200 and 5 30/60 kC tapes on the H1250 with tape switching of the two drives between the two systems. One 900 LPM printer on each with a 600 CPM card reader. The H1250 also has a 1000 CPS paper tape reader and 100 CPS punch. Both systems operate under MOD2 operating system or the multiprogramming system OS/2000.

One small H115 24K with 2 disc packs and 300 LPM and 300 CPM operating under MOD1 system is due in the next two weeks.

Hope ACC members interested in machines being released, a further release is expected January of a further 1901 and a 1902.

FOR SALE

One ICL 1901/3 16K CPU 4 peripheral controls, one 1932 600 lpm 120 pp (3 phase) printer, one 1916 1000cps paper tape reader, operators console with KSR33. Executive software system configured for this system with a cluster of four 1971 20 kC tape decks. With mainetance manual set and all

equipment castor mounted for easy removal. Needs space about 15' x 10' (with 1971's) and 3 phase power. £250 ex-site Huddersfield.

Two ICL 1500 systems 20K CPU Simultaneous Mode. Eight 10 kC tape drives (2 clusters of 4), 1000 cps paper tape reader, 600cpm, 1001pm 120pp pntr. All maintenance documentation, software FORTRAN, COBOL, RPG etc and spares.
System A is ex site Ipswich and includes a Flexowriter and 2 data prep equipments £350.
System B ex site Huddersfield with 2 data preps and one card punch £325
Both systems are available with upwards of 500 reels of 1200' ½ MT 800bpi. Both systems operational, single phase 30A 250V, require space 20' x 15'

One ICL 1500 CPU incomplete, six 30kC tape drives (7 track). Ex site Huddersfield £125

One ICL 803B (popular ACC machine !). 8K store, floating point arithmetic unit, 2 film handlers, 50 films. 1 paper tape station with two 500 cps paper tape readers and two 110cps BPR punches and data reproduction unit Creed 75. Holley (CDC) Line Printer 300 lpm 120pp. Elliott B54 card reader. High speed character printer (3 phase).Data prep unit Creed 75. Machine is single phase 250V 20A except for character printer. Needs 15' x 20' and includes maintenance documantation and full write up. Lots of spares including OC42/44 transistors, boards etc. + spare 4K CPU, film handler, power unit etc. Runs Algol 60, Autocode, BASIC(in batch mode only) and Language H (COBOL'ish). Ex site Huddersfield £250.

Jon Aslett

BUSSES *Part 2*

BUS TECHNOLOGY - SHORT BUSSES

This section considers relatively short bus systems operating at moderate speeds, namely busses up to about one metre having switching (transition) times of a few nano-seconds or greater. This covers most amateur applications for TTL or MOS connections within home-built computers. Different techniques have to be used when the signal propogation delay along the bus line is comparable with or even greater than the signal edge speed since the bus has then to be treated as a transmission line.

For short busses the design is mainly constrained by Transmitter drive capability and Receiver input loading. When the bus is fully loaded by the maximum number of transmitters & receivers the output levels produced by the transmitter should be sufficient to operate the receivers correctly, with a suitable margin for system noise immunity.

We can usefully define;

VOH as the minimum specified 'high' output voltage of a transmitter when it is driving an output current of IOH

VOL as the maximum specified 'low' output voltage of a transmitter when it is sinking an output current of IOL

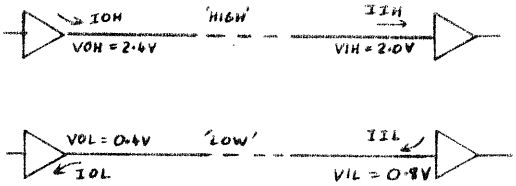
VIH as the minimum specified input voltage that any receiver will recognise as a 'high'

VIL as the maximum specified input voltage that any receiver will recognise as a 'low'

IIH as the maximum specified input current taken by a receiver when its input is at VOH

IIL as the maximum specified input current from a receiver input when it is at VOL

Thus, for standard TTL;



Note that VOH > VIL , VOL < VIL , the difference being the system noise immunity.

For some conditions (open collector outputs in the 'high' state, or tri-state logic when disabled), a bus driver is not supposed to supply output current, however, it being an imperfect world, a leakage current will flow. This is defined as IOX, the maximum leakage current that will flow in either direction when the driver output is connected to any voltage in the range VOL to VOH.

Similarly, the input circuits of some tri-state gates can be turned off, and for these IIX is defined as the maximum input current (in either direction) which would flow when the input is at any voltage in the range VOL to VOH.

Table 1 gives specification values for VOH etc. for the main types of TTL devices commonly used as bus drivers and receivers.

UNIDIRECTIONAL TTL BUSSES

One Transmitter, Many Receivers.

This is the simplest case, not requiring open collector or Tri-State gates. Examination of Table 1 gives the rules shown in Table 2.

Table 1 ; DC characteristics

		VOH Volts	VOL Volts	VIH Volts	VIL Volts	IOH mA	IOL mA	IIH mA	IIL mA	IOX mA	IIX mA	MAIN USE
Standard TTL												
normal gates	(7400)	2.4	0.4	2.0	0.8	-0.4	16	.04	1.6	-	-	R
buffers	(7440)	2.4	0.4	2.0	0.8	-1.2	48	.04	1.6	-	-	T
O/C gates	(7401)	*1	0.4	2.0	0.8	*1	16	.04	1.6	.25	-	T
O/C buffers	(7438)	*1	0.4	2.0	0.8	*1	48	.04	1.6	.25	-	T
74 L TTL												
normal gates	(74L00)	2.4	0.3	2.0	0.7	-0.1	2	.01	.18	-	-	R
O/C gates	(74L01)	*1	0.3	2.0	0.7	*1	2	.01	.18	.05	-	T
74 L S TTL												
normal gates	(74LS00)	2.7	0.5	2.0	0.8	-0.4	8	.02	.36	-	-	R
O/C gates	(74LS01)	*1	0.5	2.0	0.8	*1	8	.02	.36	.1	-	T
buffers	(74LS40)	2.7	0.5	2.0	0.8	-0.4	24	.02	.36	-	-	T
O/C buffers	(74LS38)	*1	0.5	2.0	0.8	*1	24	.02	.36	.25	-	T
Tri-State TTL												
normal gates	(DM8093/4)	2.4	0.4	2.0	0.8	-5.2	16	.04	1.6	.04	.04	T R
buffers	(DM8095-8)	2.4	0.5	2.0	0.8	-5.2	48	.04	.4	.04	-	T R

*1 external pull-up resistor needed

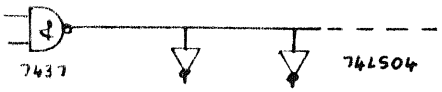
Table 2 : One Transmitter, many receivers

Transmitter	maximum number of receivers 74	74L	74LS
74 normal (7400)	10	40+	20+
74 buffer (7440)	30	120+	60+
74L gate (74L00)	1	10	5
74LS gate (74LS00)	5	40+	20
74LS buffer(74LS40)	10+	40+	20+

Note; + indicates that the maximum number of receivers is limited by the 'high' output level current driving capability of the transmitter (IOH) and the input leakage of the receivers (IIH). In a practical system one can exceed these figures slightly - alternatively a pull-up resistor will improve matters.

It can be seen from the above that standard 74 TTL buffers (7428 Quad 2 i/p NOR, 7437 Quad 2 i/p NAND, 7440 Dual 4 i/p NAND) make the best transmitters for a general purpose bus, although normal TTL gates (7400, 7404 etc.) may be used where their restricted capability is sufficient.

Receivers may be standard 74 TTL or, preferably, 74L or 74LS. Of the latter two, 74LS (Low Power Schottky) is better although at present rather more difficult to obtain cheaply.

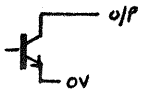


UNIDIRECTIONAL BUSSES

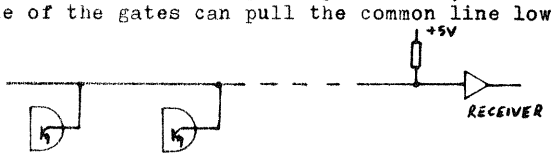
Many Transmitters - One Receiver

Using Open Collector Gates

In 'open collector' gates (7401,03,09,12,22 etc.) and buffers (7416,17,38) the output stage consists of a single transistor, the normal TTL 'totem pole' pull-up circuit being omitted.



If the outputs of a number of these gates are connected to a common bus line which is also connected to a receiving gate input and a suitable pull-up resistor, then any one of the gates can pull the common line low;

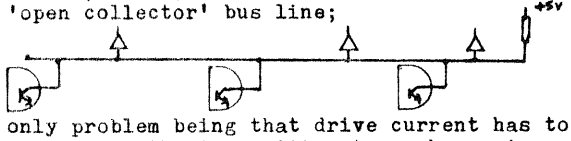


The pull-up resistor should be as low as possible to reduce propogation delays and to counteract the transmitter output stage leakage currents (IOX) when the bus is in the high state, but the resistor has a minimum value determined by the IOL rating of the transmitters. Optimum values for the pull-ups, when the receiver is a single gate of the same logic family as the transmitters, are given in Table 3.

BIDIRECTIONAL BUSSES

Using Open Collector Gates

Instead of the single receiver shown in the previous section, multiple receivers may be connected to an 'open collector' bus line;



The only problem being that drive current has to be supplied from the transmitter to each receiver, and therefore the minimum value of the pull-up resistor has to be increased for every added receiver, which in turn reduces the possible number of transmitters.

There is therefore a trade-off between the allowable number of receivers and transmitters and the value of the pull-up resistor, as determined by the equations;

$$R > \frac{5 - VOL}{IOL - IIL \times NI}$$

$$R < \frac{5 - VOH}{IOX \times NT + IIH \times NI}$$

where NT = number of transmitters
NI = number of receivers

Typically 7 transmitters and 7 receivers can be connected, although this can be improved by using different logic families for the transmitters and receivers and/or using open collector buffers for the transmitters. A useful combination results from 7401/3 transmitters, 74LS receivers, and 560 ohm pull-up resistors. This allows up to 20 transmitters and 20 receivers to be connected.

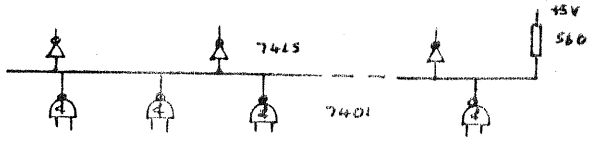


table 3 : pull-up resistors for open collector bus with one receiver

Logic family	Res (Ohms)	Max no. of transmitters
normal 74 (e.g.7401)	330	30
74 buffer (e.g.7438)	100	100
normal 74L(e.g.74L01)	2.7K	20
normal 74LS (74LS01)	620	40
74LS buffers(74LS38)	220	45

In practice one would rarely need more than about 20 transmitters on a bus (if you do then have a hard rethink about the basic system design) so normal 74 or 74LS gates would be adequate. 74L is not really recommended except for very small busses as the pull-up resistor is rather too high to give reasonably short propogation delays on long busses with a lot of capacitance.

to be continued

ED'S BIT

Quote of the week must come from the D.Cosserat, D.England & Partners State of the Art report 'Microprocessors';

"At the present time there is actually a significant number of homes which do not contain a single computer. This situation is unlikely to last for very long."

ACC membership has now reached 520, and at the present growth rate can be eapected to reach 600 by the end of the ACC year. This figure compares with 209 for 1973/4, 282 for 1974/5 and 405 at the end of last year. And tomorrow the world !!

Based on members' letters, the ACC committee has decided that the ACC VDU project will be dropped, as although the PW & ETI designs are not perfect, they are workable. We will, however, welcome ideas for improvements & modifications on these basic designs.

We are somewhat suprised at the continuing interest in the WB, and possible upgrading to a WB-2, in view of the availability of MPU. But as has been pointed out, half of the fun is in the building, and connecting up a few anonymous packs doesn't give much cause for pride. Thus, if anyone is seriously prepared to work on the design of a WB-2, would they please get in touch.

A fundamental problem facing any designer, and of particular importance to the amateur computer hack, arises from too much freedom. Take for example the choice of an MPU, there are at least 20 types available, most of which would be adequate, each offering some advantages and some disadvantages to the user. Since the design of hard and software for any reasonable computer system represents a considerable manpower investment, it must make sense to restrict one's choice by some form of standardisation. Therefore the ACC committee has adopted the policy of supporting those designs which look like being useable as a standard (although that doesn't mean that the newsletter won't publish non-standard ideas !). Thus, if it looks at all promising, the ETI system 68 will be supported.

We are still short of software oriented articles, at any level, contributions please.

mike lord

MPU NEWS

The DataGeneral MicroNova 16 bit MPU and associated chips are now available, at £160 for the MN601 MPU, £71 for the MN603 I/O controller.

GEC have released an 8 bit binary multiplier chip, MA8807A, which is designed to be compatible with the 8080A CPU. Multiplication time is 5uS, small quantity price around £8.50.

Ferranti have developed a 16 bit bipolar MPU, the F100L (does anyone have any data on this that they could lend me ? ed)

Intel has published the 1976 version of their data catalogue; £1.50 from distributors.

Mostek are now selling a 16K bit dynamic RAM - the MK4116P - for £60 (one off price).

SERT 'MICROPROCESSORS AT WORK' SYMPOSIUM

A bound copy of the papers presented at the symposium is available at £7 from 'Society of Electronic & Radio Technicians', Faraday House, 8-10 Charing Cross Rd, London WC2H OHP.

PLAYING WITH YOUR COMPUTER

COMPUTER MUSIC NOTES

THE SYNTHESIS OF MUSIC & SPEECH
P.M.Woodward Comp.J. 9,257 (1966)

THE TECHNOLOGY OF COMPUTER MUSIC
M.V.Mathews MIT Press

INFORMATION THEORY & MUSIC
R.C.Pinkerton Scientific American 194 No 2 1956

THE COMPUTER AND MUSIC
H.B.Lincoln Cornell University Press (1970)

MUSIC BY COMPUTERS
Foerster, H.Von & Beauchamp Wiley 1969

EXPERIMENTAL MUSIC
L.A.Hiller & Isaacson McGraw-Hill 1959

COMPOSING MUSIC USING A NOVA 1210
L Shakeshaft Computer Education No 18,9 (1974)

FROM MOZART TO THE BAGPIPE WITH A SMALL COMPUTER

T.H.O'Beirne 'Bulletin of the Institute of Mathematics and its Applications' Vol 7 No 1 Jan 1971

SHOP

WANTED

Required for schools--any old hardware for demonstration and teaching, e.g. disc cartridges, core memory, PDP-8's, ... anything, any condition. Offers, in the first instance, to: Mr. R. Cole, Maths Dept., South Bank Polytechnic, Borough Road, London S.E.1.

WANTED

Disc or Drum, less than £150. Preferably in working order.
E.A.Greene 23 St Peters St.,S.Croydon CR2 7BG

FOR SALE

IBM I/O printer (golfball type) very neat appearance. As advertised by Keytronics for £100. Complete with original IBM illustrated service manual, over 200 pages (not photo copies). 50 way plug/socket also provided. Needs slight attention, the spring return seems to be loose, otherwise OK. Must sell, space needed. Offers around £50 or will consider exchange for communications receiver (but not ex govt).
J.J.Smith 7 Kettlebaston Rd.,Leyton, London E10 7PE
home ; 01 556 3368

A ready assembled UHF modulator is available, ready assembled, from Crofton Electronics Ltd, 35 Grosvenor Rd, Twickenham,Middlesex @ £8.76 + £1.24 for P&P & VAT.

Computer Workshop , 174 Ifield Rd, London SW10 9AQ, tel; 01 373 8571 are selling a computer kit based on the 6800. £316 including 2K of RAM, cabinet, control interface and power supply.
They also sell the AC30 audio cassette interface, for storing data on a cassette recorder at the standard 300 baud, at £65 in kit form.

'Introduction To Microprocessors' Splits

Adam Osborne's book 'An Introduction to Microprocessors', mentioned on page 3 of the August Newsletter has sold out and is now being published in two (expanded) volumes;
Vol 1 ; Basic Concepts.
Vol 2 ; Some Real Products.Covers every major microcomputer and major chip slices.
$7.50 + $2.50 airmail each from
Osborne & Associates Inc.
PO Box 2036, Berkeley, Ca 94702 USA

BYTE

Some ACC members will have received a free copy of this magazine, but for those who haven't it is a glossy magazine, about 100 pages, published each month in the USA since September 1975. Excellent reading for the amateur computer enthusiast, recent issues included the following articles;
'Build a fast cassette interface unit'
'Machine Language programming for the 8008'
'Build a TV readout device for your microprocessor'
'Zilog Z80'
'A basic Star Trek trainer'
'AMSAT 8080 debug monitor'

Available by direct subscription to Byte Publications Inc, 70 Main St., Peterborough, New Hampshire 03458 USA @ $12 per year
Or from European Distributors;
J Remizo, 142 Grove Lane, Hale, Altrincham, Cheshire @ £10 /year.
PACS Ltd., Frankfurter Strasse 78, D61 Darmstadt, West Germany @ DM 45 /year.

LOCAL GROUPS

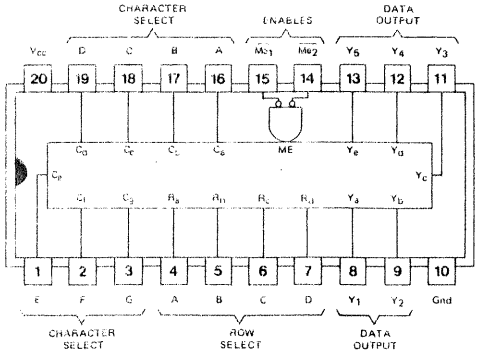
The Electronic Organ Constructors Society Midlands Section holds meetings at my house 5 times a year, any ACC members who are interested would be very welcome. In fact if there are enough ACC members in the midlands interested in a separate get together to talk computers I would be happy to house such a meeting.
Roy Diamond
27 Loweswater Rd., Coventry CV3 2HJ (Cov 454061)

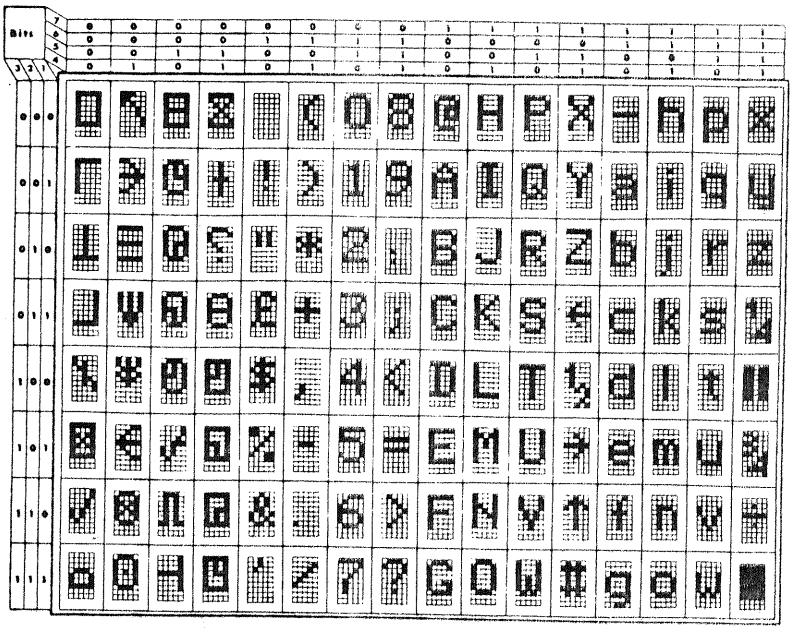
IRISH GET-TOGETHER

About seven of us got together and had a pleasant evening swapping bits until it was so late that we nearly didn't get into the pub. One member brought along his pet 4004 which he keeps in a shoe box. He let it out of its box and we all patted it and watched it blinking at us. At the moment he feeds it bunches of diodes to make it do tricks (one 16 pin plug + diodes = one 8 bit instruction, he keeps the instructions in a bag and pops them into a row of 16 pin DIL sockets when he wants it to do a trick but he's building another box to help it remember harder tricks (RAM + switches for loading)).
Two members are going to buy a 6800 kit to teach their pupils with, and some members are allowed to play with their company's mascot when everyone else has gone home. Otherwise there seems to be a great shortage of pets in Ireland.

Tiger Tom

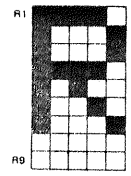
Texas Instruments SN74S262N
ROW OUTPUT CHARACTER GENERATOR





ROW SELECT TRUTH TABLE

ROW SELECT				SELECTS ROW
R_d	R_c	R_b	R_a	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	Data Outputs Forced to Logical '0'
to				
1	1	1	1	



electrical characteristics over recommended free air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH} High level input voltage			2			V
V_{IL} Low level input voltage					0.8	V
V_{OH} High level output voltage	V_{IH} = 2V, I_{OH} = 0.2mA	V_{CC} = MIN, V_{IL} = 0.8V	2.7	3.4		V
V_{OL} Low level output voltage	V_{IH} = 2V, I_{OL} = 4mA	V_{CC} = MIN, V_{IL} = 0.8V			0.5	V
I_{IH} High level input current	V_{CC} = MAX	V_I = 2.7V			20	µA
I_{IL} Low level input current	V_{CC} = MAX	V_I = 0.4V			-360	µA
Output leakage	V_O = 2.7V	V_{IL} = 0.8V, V_{IH} = 2V		20		µA
I_{CC} Supply current	V_{CC} = 5.0V			50		mA
Access time	Worst part.			200	260	ns

features

- Static operation
- 5760 bit capacity
- 128 characters of 45 bits (5x9)
- 7 input character decoder
- 4 input row decoder
- Character format chosen to allow rounding on all characters
- High speed – 280ns character access time
- Lower power – 250mW
- Single + 5V supply
- 2 enable inputs for system expansion
- 20 pin DIL N-pack
- Compatible with most TTL and DTL logic circuits

LETTERS

I am poised on the brink of constructing the WB-1 but hesitate for the lack of a reasonable interface e.g. V24 ASCII, and that its directly accessable memory is only 256 bytes. If anybody has a proven, hygenic method of dealing with either limitation would they please publish or contact me.
Tim Moore 24 College Rd, Maidenhead, Berks SL6 6BN (0628 29073)

I have surplus to my requirements one 6800 kit all made up and working. I also have a complete set of blurb on the Intel 3000 series bit slice chips and a machine using them (almost working). I would stronglr recommend anyone who is thinking of using them to get in touch with me first.
If anyone is interested in a portable software project would they like to phone me, at home, and I'll try to arrange something.
J Florentin 17A Campden Hill Gdns,London W8 7AX
tel; 01 229 0859

Regarding the ACC VDU, I feel that another design would be superflous after the ETI design. Parhaps ACCN could carry articles on mods and improvements e.g. more lines, graphics etc. Other peripherals would be interesting and the speech synthesisers in BYTE No 12 look fascinating.

P M Jessop

Could I recommend "Design of Digital Systems", advertised in many electronics magazines, for anyone such as myself who is a newcomer to digital electronics.

D A Robinson

VDU ; I agree there is little point in developing an ACC VDU in view of the availability of other models.

FUTURE OF NEWSLETTER ; I agree on drift away from big constructional projects, but see an ongoing need for;

a) simple circuits, interfaces, modifications to published circuits etc.

b) contact between members. I would think you should set a target of getting from each member at least once a year (perhaps on a pre-printed form at subscription time) a brief summary of where he's at, where he's going, what equipment he has running etc. You could then publish a summary.

c) practical info of educational type and interesting news.

One of my problems is that I keep coming across references to codes & interface standards which I don't know. I can generally work out what sort of thing it is, but don't know where to go for the details. Some of the standards I've come across recently were;

ASCII - is it a 7 bit code , should there be a parity bit ?

TTY interface /20 mA current loop - what are the specifications for voltage, current, timing etc. I'm sure I could design a TTY/ASCII converter if I knew where to begin.

RS232 & RS232C

EBDIC code

Tiger Tom

As I am a radio amateur would you please add my call sign to the list.
R A Rimmel G3RQS

VDU

Some items of positive information for VDU constructors;

1) Theory would indicate that about 55 to 65 characters can be displayed on a monochrome TV. In practice the resolution is adequate for 80 - useable quality but not startling.

2) A UHF modulator can be easily constructed for under £2 using a ELC1043/05 varicap tuner (salvaged) as supplied by Manor Supplies, 172 Westend Lane, NW6. The modifications are described by E. Trundle in Practical Television April 1975 page 251 and Feb 76 page 210. I know of four separate successful constructions.

T W Moore

WB

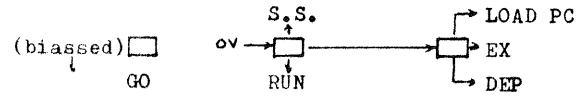
Just a letter to let you know I have finished my WB and a few comments on it.

I made it on 3 boards 9" x 5" of PC board drilled to fit the ICs with holes by most used pins - very few PC interconnections except for all power. I used 74100 in place of the 7475 as they were available. Most IC were ex computer boards or from "200 IC at £1.20 untested" - all checked before reuse. The only faults were 2 IC (both new !) and 1 poorly soldered joint.

The PC boards (and front panel) are connected by 2 x 32 way 0.15" connectors, the sockets are surplus and the plugs are gold plated cut from old computer boards and Araldited to the end of my PC boards.

The power supply refused to stabilise off load (perhaps transistor leakage as I was using cheap transistors) so I used a 723 + 2N3055 and your crowbar.

My front panel uses keyswitches in place of your rotary and is connected;



Which seems simpler than a rotary.

When wiring I found it a help to have a wiring list for S I C connections e.g. IO to 2o, 42.1, 45.4 S5 etc. missing connections otherwise found by an empty hole by an IC.

Anyway it works very well - I am intrigued by its speed and have coupled it to a Ferranti TR5 reader and a Creed 5 hole punch with very little trouble apart from its speed (Ferranti) and interference (Creed).

Future ; I think WB2 is probably a better bet than a VDU as both ETI and PW have designs and even the WW Teletext decoder is useful. Snags with WB 1 to WB 2 conversion seems to be partly the use of low memories internally unless they are used for this on each page.

There is probably a demand for suitable instruction strings to perform arithmetic operations e.g. + - x etc. taking acount of decimal point - has anyone done it with only 256 instr ?.

A H Yorke

Concerning the 'Buses' article;

1) It is incorrect to say that the PDP11 has a 'Controller' on the bus separate from the CPU and the peripherals. The determination of which device (only one) becomes bus master is done by logic inside the CPU, not in a separate device. Hence it is incorrect to say it is possible to have no CPU on the bus, as the bus simply would not function.

2) It is true to say that a bus structure reduces the data handling capacity of a machine compared to a 'direct channel' machine. However, whether it reduces the capacity slightly (as said in the article) or greatly depends upon the sophistication of the machine. The ICL 1900 has bussed data lines but is much faster than the PDP11. This is because the ICL 1900 uses special data transfer instructions in a ROM whereas the PDP 11 uses ordinary prog instructions in the ordinary core store.

With regard to other things;

It would surely be a waste of time to pursue the design of a VDU when there already exist a number of designs and kits (but I am biassed as I am not very interested in a VDU anyway).

What I would like to see pursued is the construction of a reasonably useful mini comp. By this I mean the following;

1) Pursue and complete the design of WB2 i.e the extension of WB1 to 16 bit /64k.

2) Extend WB2 hardware wize i.e. hardware multipliers etc.

3) Extend WB2 software wise i.e. assemblers etc.

Number 1 I admit would be difficult, but once it is done numbers 2 & 3 would provide opportunities for members to correspond to the ACCN with ideas & designs, like the correspondence over the cassette storage devices.

Which way the ACCN (and the ACC) ?

The ACCN suffers at the moment from the lack of any definite activities by the ACC. When WB1 was 'going on' there was no problem about the contents of the ACCN, or the direction of the ACC. The lack of ideas about another project leaves a void in the ACCN. Perhaps some interesting articles might be submitted on the question ; why is it impossible to build a machine to play good chess ? (or can someone come up with such a machine ?).

Knowing now how many people have built / are building WB1, it would be interesting to know how many people have got / soon will have a working mini set up.

R H Stopford

I have been reading through back issues of ACCN and expect to build WB1 later this year. I think some people have been snowballed (brainwashed ?) by all this microprocessor stuff and I think they have forgotten what this computer hobby is all about.

I am all for technological advances but when it comes to actually learning something far better to build say the Weeny Bitter, get it working, modify it, change it about, add more memory etc. then upgrade to a more powerful system.

I would like the ACC to continue in development of WB2 using normal TTL devices - so what if it does cost another £30 - £40 - far better than connecting up an anonymous box (microprocessor) which is encapsulated and cannot be modified. Remember too that people have a junk box with TTL devices in it these days which will reduce the actual outlay. Another thing about using TTL devices is that if you use sockets or soldercon pins they are re-useable. I know this is stating the obvious but the point I am getting at is if you have constructed say a teletennis unit or other item which uses TTL in sockets you can whip them out and use them to extend WB 1 or WB 2, and maybe one day WB 3.

I know nothing about software at the moment and hope to learn about this through ACCN, and when it is built I hope to add CUTS to the WB. At present I am building the ASCII keyboard per recent ACCN using the suggested Greenweld keys (ex calculator keyboards).

Assuming WB 1 and CUTS are built (and work) the next thing that might be added would be a VDU.

Having read about the PW and ETI and WW Teletext and a couple of American systems it seems to me that no real standard exists. I would like to see ACC proceed with its own VDU project (but not at the expense of WB2). Thinking about compatibility I suggest the same characters per line and number of lines as Teletext be used. As most people have B/W UHF TV's these days I expect most would like to use these for readout by using a plug in modulator. If the set is rented (or even if it is not) I don't think its advisable to poke around inside the set (EHT does not sound very TTL compatible to me !).

J J Smith

TERMINAL

Re W.G.Beers comments about cheap terminals- I have found an easier alternative - BRASS NAILS !. About 13mm long sold by the ounce at the local hardware or DIY store. Great for veroboard as you simply push through hole with pliers and solder head to copper (cut off the sharp point). Cheaper than vero pins and quicker than bending up bits of wire.

J J Smith

SYNTH

I am attempting to interface my synthesiser with an MPU (probably the 6800) and would be interested to hear from anyone who has attempted anything similar or has any ideas about software / hardware for such a system.
M McLean 19 Haldane Ave, Haddington, E.Lothian

TREK

I am writing a new, ultra sophisticated (structured even) version of the world famous STAR TREK program and would like a little help. Would anyone who has any comments, suggestions, listings of previous or planned versions etc. please contact me.
p.s. anyone interested in forming a Star Trek Fan Club in the UK ?

After much trial and error (mostly error) I have come up with an extended set of rules for LIFE. These rules allow the user to generate pretty coloured patterns, and are as follows;

1) Decide which colours you want, assign one to the 'dead' cells (background) and the rest to the 'live' cells. Count the number of 'live ' colours. Call this N.

2) New-born cells are always numbered 1, 'dead' cells are always 0. Cells which survive have their number (1 to N) defined as follows; Add together the cell number and the numbers of all its neighbours divide by N and, taking the remainder, add 1. Thus in the following pattern (N=4):

```
1 0 2
3 4 0
0 0 0
```

the centre cell, at the next generation, would be a 3 (1+2+3+4=10 ; 10/4=2 ; r=2 ; 2+1=3)

I have devised (yet another !) method of recording data on tape. My system is tentatively called PITS (Phase-coded Interchangeable Tape System), is for stereo machines and works as follows;
Each bit is recorded as a note of a certain frequency (virtually any frequency will do - in fact PITS can be used, say, to record a tape at 75 baud and replay it at 300 baud) such that the two channels are in phase for a 1 and in anti-phase for a 0. To read the tape you need a channel sum detector and a channel difference detector. If you get an output from the sum detector the bit is a 1, if from the difference detector, the bit is a 0, if both then it is a recording error, if neither it's the interbit gap. I'm not sure what the tape format would be, but I think it would be a good idea to record each character as 12 bits (8 code, 4 parity) in order to facilitate error detection and correction.

Recent meetings; I felt that the DEC gig was not as good as last time but the EMS gig was excellent. Pity that Alan Sutcliffe could not demonstrate any of the audio devices (I would have liked to have heard a demo of the Vocoder - especially since hearing the 'Walter Carlos Clockwork Orange' album) but this was amply compensated for by the demonstration of the EMS 'Spectre' video synthesiser. Alan showed us several weird and colourful effects, some of which are used on 'Top of the Pops' and other programmes. I took some photographs of the results using the well-known professional light-metering technique of setting the shutter speed and aperture and saying a quick prayer. Somehow the technique worked.

R J Baker

MINE 6800

The system I have going at the moment is based on a 6800 processor, although it uses a PDP-11 type of bus structure, which is designed to be compatible with almost any CPU architecture from 8 or 9 bit bytes to 16 or 18 bit words. The hardware which is now running consists of a processor, 16k of 1 uSec core memory, 2 ASCII electronic keyboards, 2 visual displays, paper tape reader and punch, Datel 200 modem, and multi-band RTTY interfaces.
The VDUs are basically similar, but one is 13 rows only, whereas the other has 20 rows of 80 characters bidirectional scrolling, matrix graphics and 7 display colours. Although I can supply information on these if requested, I would not recommend this particular design to anyone thinking of constructing a VDU. This is because they were designed by me 3 years ago, when dynamic shift registers were the only form of cheap storage available. With modern RAMs one could achieve the same facilities far more easily.
One printer I have is a Creed 75 modified to ASCII. This involved removing the type and replacing it in a different order, plus quite a lot of mechanical mods, and is again not a method recommended to the faint of heart. The other printer is from an IBM 2741 terminal. The problem with these seems to be that the ASCII to Selectric code converter chips available do not provide for all characters, and therefore I ended up blowing an ultraviolet PROM to meet the particular machine's requirements.
The system has a console which acts as an autonomous device on the Bus, thus it can be used without reference to the CPU. There is a provision for starting from a manually set address by causing the console switches to be read by a reference to the top 2 bytes in the memory space. Similarly, a vectored priority interrupt scheme has been implemented by making a reference to the interrupt location in high memory by the processor send an acknowledge signal down the bus. The highest priority device which is requesting service responds by asserting its own vector location in low memory, and thus device polling is avoided. The non-maskable interrupt is being used only for power failure recovery.

Applications which I have in mind at the present are mainly in the area of communications handling and text processing, so a byte structured system is ideal. In particular I am starting to use the machine as a sophisticated aid to radio-teletype operation, and as a useful front end on line to time-sharing networks. I should soon have facilities to tune the radio equipment under program control by means of DACs, and I am planning to interface my Teletext decoder (which is an independent unit) to the bus as a further data source.
I also have thoughts about making the frame store of a slow-scan TV (128 or 256 line) standards converter accessible to the processor, which would allow not only the generation of electronic pictures and captions, but the application of noise reduction algorithms to incoming pictures to improve their quality. The frustrating fact about SSTV though, is the simplicity of the pulse standards, and the wide variations in signals received. This tends to limit the possibilities of digital improvement.

Martin Allard

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