AMATEUR COMPUTER CLUB NEWSLETTER

VOLUME 5 ISSUE 3 AUGUST 1977

HERE COME THE BIG GUYS

Now is where it really starts. Computers for everyone. Pouring out of the factories, spilling across the land, TV commercials before Christmas, cut-price offers after. 'Which' reports detailing the number of (100 gm) operations before the keyboard starts to stutter. Well worn machines in Oxfam shops. It will all happen. The small computer market is about to break wide open.

Because, you see, the big boys have arrived on the scene. Heath,Tandy, Commodore; they're all busy announcing/leaking details of their new products. And they'll have spent real money researching the needs of the market, and more money designing their products to meet those needs, and they'll spend a lot more promoting their machines so that no-one who might possibly buy one is unaware of what they have to offer.

But the real break is going to be price. and here firms like Commodore have the financial muscle to go for the big volumes that bring the price down, which in turn generates the high sales volume.It's the Model T phenomena, and one can draw parallels; a lot of people will buy machines purely for fun, once the price is right, without really knowing what they will do with them - but uses will evolve as users play; some practical, some for pure amusement (could Ford have envisaged stock car racing- I suspect that it would have been viewed almost as sacrilege in those days). In 5-10 year's time we'll look back with amused affection on these primordal machines. But they will have made the break-through and that's what counts.

The Tandy TRS-80 is now on sale in the USA, and it is hoped that it will be in the UK early next year. It is an assembled system using a Z-80 with 4k RAM, 4k ROM, keyboard, VDU screen, cassette recorder & a BASIC interpreter. Price is expected to be in the £400 - £450 range.

Although Heath are keeping a low profile in the UK for the moment (see letter on this page),they have announced two computer kits in the States. The H8 is an 8 bit machine built around the 8080 with the now almost obligatory hex keyboard & seven segment display driven by a 1k ROM monitor. Interestingly, it does not use the S100 bus, but does provide a cassette tape interface using the Kansas City (CUTS) standard. $375, 8k memory $235 extra. The H11 is more interesting since this is basically a DEC LSI-11 suitably packaged and therefore uses DEC's PDP 11/03 bus structure. $1295 with 4k of memory. Both computers come with software, including BASIC, assembler, editor and debug programs. Heath are also bringing out a complete VDU kit ($530) and a paper tape reader-punch ($350).

Commodore's PET 2001 is selling so well in the USA (rumour has that demand has already outstripped the planned production capacity of 1000 a day !) that it may be several months before it appears in Europe.When it does, UK price is expected to be around £500. One significant feature is that it has provision for working with the IEEE/IEC bus - this is an asynchronous 8 bit parallel bus structure originally developed by H-P for linking programmable instruments and controllers together (I'd welcome an article on it for the ACCN ed).

And of course these machines are not only intended for amateurs. The really big market is going to be in small businesses and small departments of big businesses. I remember a few years ago the quality department of the firm I'm with bought one of the H-P machines, I forget the type but it was about equivalent to the PET; programmed in BASIC it had it's own keyboard and alphanumeric display, and at that time cost several thousand pounds. The department had a bit of a struggle to get permission to buy it because they had to financially justify the investment (as well as prove that they couldn't get the flexibility they needed from the site 360), and they didn't forsee enough work to keep it anywhere near 100% occupied. Now, with machines like PET costing not much more than an office typewriter, it'll be almost worth having one in every office, even if it's used for only an hour a day.

IN THIS ISSUE

BITS & BOOZE

As meetings seem to be few and far between at the moment may I suggest an evening in the pub. I will be pleased to see all and sundry in the 'Smugglers' Warren St. (near Warren St. tube station) from 6.30 onwards on Thursday 22nd September.

Jef Cole

A LITTLE LETTER FROM HEATH

Dear Sirs;
Thank you for your letter of the 9th August 1977 requesting information on our Computers.
We regret that we have not yet had detailed information from our Parent Company in the United States on these products but we are not introducing them in the United Kingdom until May 1978. As soon as we have detailed information on them we shall be pleased to send it to you. Thank you for your interest.

Yours faithfully
for Heath (Gloucester) Limited
E.J.Dethridge General Manager.

PET USER GROUP

A user group has been formed for people interested in the Commodore PET 2001 Computer.

The PET is a compact computer with integrated keyboard, CRT with character and graphics capability, cassette drive, 14k ROM operating system including full 8k BASIC, and 4k RAM user space. The PET will provide exceptional computing value with a complete price of $595.

The purpose of the PET User Group will be to share and exchange applications, programs, and hardware expansion techniques, and to provide general user feedback.

The first year membership is $5.00 (add $5 for overseas air mail) and will include the User Notes publication.

Pet User Group PO Box 371,Montgomeryville,PA 18936

SHOP

FOR SALE

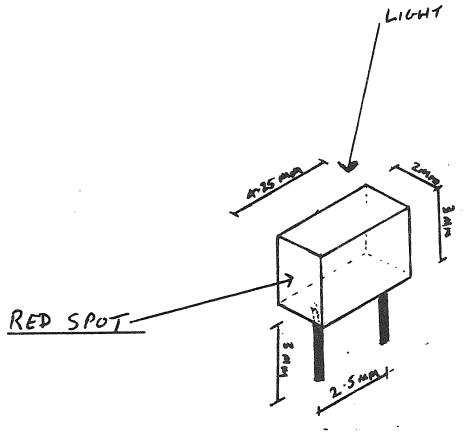
1) KSR33, only one hour since new but e/magnet driver pcb missing, manuals available. £140 (ASCII coding of course).
2) Olivetti 349 ASR. ASCII coding, upper & lower case printing with all electronics & data. Beautiful condition. £250.
3) Teletype high speed tape punch, 5 level. Free to anyone who can come and get it.
4) Viatron System 21. Microprocessor system with keyboard, VDU, cassette tape store, and also ½ inch mag tape unit. All very compact, working with all manuals. £600 the lot, with stack of spares.

I also have a huge stock of old computer gear - and invite anyone interested in spares to contact me. Lots of items (ie old core stores) very cheap or some items free. Nearly all 7400 series TTL available. For anyone with a Cossor VDU I have a spare monoscope tube.

Nigel Dunn 21 Campion Rd.,Widmer End,High Wycombe, Bucks. tel; (weekends only) 049 47 4483

WANTED

One photocell to fit a read head removed from an Elliot paper tape reader type No T10/200
Ken Horton 50 Lymefield Drive,Worsley,Manchester M28 4WA tel; 061 228 6333 ext 372 (day) or 061 799 0192 (evenings)



SALE

I have found a source of cheap (approx £18) type 2708 1k x 8 EPROMs. G.E.Parker, 19 Cox's Close, Bedford MK40 4JZ tel;(0234) 57373 (evenings).

FOR SALE

Plessey 'atlas' 12k core store with drive, sense and inhibit wires. Complete with full technical data £30.00

Electric 5 hole paper tape hand punch. Old but works well £5.00

Creed 92 5 hole paper tape reader, working and in good condition, with technical data £7.00

Buyer collects
Simon Garth 67 De Parys Ave., Bedford

SALE

Over expansion forces sale of following;
Unencoded TTY Kbd £20-
ETI ASCII PCB & HD0165 £10-
MOSTEK F8 evaluation kit £90-
S100 4k RAM boards £85-
Heathkit HW-8 £110-
S100 motherboard, 15 slots with 5 connectors £70-
S100 edge connectors £5-
Ken Talbot 33 Easter Livilands, St. Ninians, Stirling FK7 0BQ Tel; Stirling 70126 (home), 70440 (office) or Falkirk 31931 (office).

WANTED

ASR33 Teletype or any other 8 bit code teleprinter, also up to 4k of 8(or 9) bit core with all the electronics.
Nigel Trewartha Neugartenstrasse 33, D-7759 Hagnau/Bodensee, West Germany.

SALE

Low Voltage Transformers. Pairs of 2N3055's on heatsinks. Regulator chips. Monster capacitors. 16k x 8 (or 8k x 16) MOS memories (400nS cycle). 12k x 13 bit core mem complete with electronics (3.6uS cycle). 5'6" 19" rack on castors. Large numbers of connectors inc D types and PCB edge ones. Switches, Lamps etc. Plug in Veroboard (reuseable) & edge connectors. Disc drive and discs (500k bytes per side). Paper tape reader. I would like to get hold of Intel 3000 series chips.
John Florentin 17A Campden Hill Gdns.,London W8 7AX tel; 229 0859

WANTED

CT1024 or equivalent keyboard & TV display driver.
Brian Lewis 7 Boughton Lane, Maidstone, Kent.

TREKFILE 'Surak'

Now at last, what you've all been waiting for, some actual code. The two modules this month are to achieve intermodule GOSUBs and RETURNs, which will be nestable up to 12 deep. Module GOSUB is as follows;

```
10 COM G0,G$(72),G(12),M0,M$(6),N0,N$(7)
20 G0=G0+1:IF G0>12 THEN (PRINT "GOSUBS NESTED 13
       DEEP":STOP)
30 G(G0)=M0:G$(6*G0-5,6*G0)=M$:CHAIN N$,N0
       !PUSH STACK AND GOSUB.
```

And as an example of how to use GOSUB;

```
10 COM as before
20 M0=500:M$="GSUBEX" !NAME AND LINE NO. FOR RETURN.
30 N0=2300:N$="$SUBREX"!NAME/LINE OF CALLED MODULE.
40 CHAIN "GOSUB"      !DO THE GOSUB.
50 !REST OF MODULE
```

RETURN is as follows;

```
10 COM ...
20 IF G0<1 THEN (PRINT "RETURN WITH NO ACTIVE
       GOSUB":STOP)
30 N$=G$(6*G0-5,6*G0):N0=G(G0)
40 IF N0<0 THEN (N0=ABS(N0):N$="$",N$)
50 ! NOTE: -VE RETURN ADDRESS DENOTES CALL FROM
       LIBRARY ($) MODULE.
60 G0=G0-1:CHAIN N$,N0 !POP STACK & RETURN
```

And as for how to use it - simple CHAIN"RETURN"

HELP

I would welcome technical information on;
1) Keyboard for VDU, ICL type 7181/9, Serial No. 2048, it has three sets of keys, four LED indicator lamps and has a lead terminated by a miniature 50-way female Cannon socket.
2) Power Supply (adjustable) 6V @ 25A. A 19 inch rack mounted supply, has a blue & silver label marked Exchange Unit ICL Part No 65-85524, Serial No 3183.
3) Rotating Magnetic Memory Drum Model No 1004-S, Serial No 1205, Diameter 10", 128 tracks, 2865 rpm 220V induction motor, made by Vermont Research Corporation, USA.

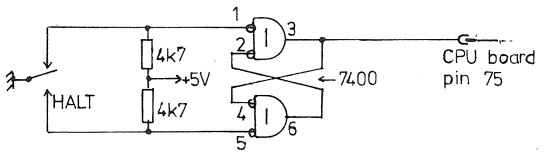
J M Baron 27 Wises Lane, Borden, Sittingbourne, Kent. tel; Sittingbourne 70160

HELP

I Have recently obtained a NCR key to tape unit No 736-101 made by Mohawk Data Sciences in the USA and imported by NCR, for which I have the reference manual and operators manual but no technical manual. The unit is believed to be complete but has been dismantled, so I would be grateful to hear from anybody with technical details as I would like to see it working again.
N K Wright 25 Penny Park Lane, Coventry CV6 2GU

7768 MICROCOMPUTER

Users have found that operation of the HALT switch sometimes corrupts the contents of memory. This is believed to be due to switch contact bounce causing the 'halt' condition to be removed for very short periods, and examination of the 6800 operation under these conditions (see the 6800 timing diagrams for Single Instruction operation) shows that it is possible for the MPU to perform a 'Write' while the Halt & BA lines are both low. The cure is to change the HALT switch for a single pole change-over type and add an external de-bounce bistable;



PUZZLE — P Rutherford

When is one half of ten equal to five, but one half of nine equals four, one half of eleven is six, and one half of twelve is seven ?

Answer on page 12

6800 LIBRARY

The library is thriving with about 200 transactions to date, having loaned about 1000 items of information. The latest index is now available (1st August 1977). It is regretted that owing to the cost of printing a small charge has been levied of two 9p stamps for the index if it is retained. There are now 136 items in the hardware and 63 in the software section and 22 in a new section dealing with operator to computer interfaces. More software is in the process of being purchased so if you have any suggestions please let me know. For those who wish to use this free service please send 32p in stamps (surplus refunded) & an A4 SAE to Tim Moore 24 College Rd, Maidenhead, Berks SL6 6BN tel;0628 29073

WB-1 & 77-68 USER GROUPS

The first WB-1 User Group newsletter has been circulated. Its a free service and has definite benefits for anybody who is thinking of, or who has constructed this TTL microcomputer, as it holds various designs for extending its memory, games software, etc.

It is hoped to distribute the first 77-68 User Group newsletter in early September, so if you want to be included in the register of users please contact Tim Moore 24 College Rd.,Maidenhead,Berks.

HEX TO CHARACTER CONVERTER

This circuit element is particularly useful in conjunction with a VDU & MPU, for a 'program debug' mode. It will automatically convert groups of four bits into the hex representation, that is the characters

0 1 2 3 4 5 6 7 8 9 A B C D E F

Operation is as follows; six is added to the input. If no carry is generated the input is less than 10 (A), and it is passed to the output. The two most significant bits of the six bit output are forced to '1'. With a 2513 character generator, this gives the characters 0-9. If a carry is generated, one more is added (by changing the state of the carry input (pin 13). Note that pin 11, the B0 input, could be used instead). The input -9 (plus 7,mod 16) is now passed to the output with the two msb's forced low, giving characters A-F.

Two versions are shown; Fig 1 for active-high input, Fig 2 (the cheaper one) for active-low input. The insert in Fig 1 shows a modification for conversion from Hex to the ICL 1900 series internal character code.

O F Morgan

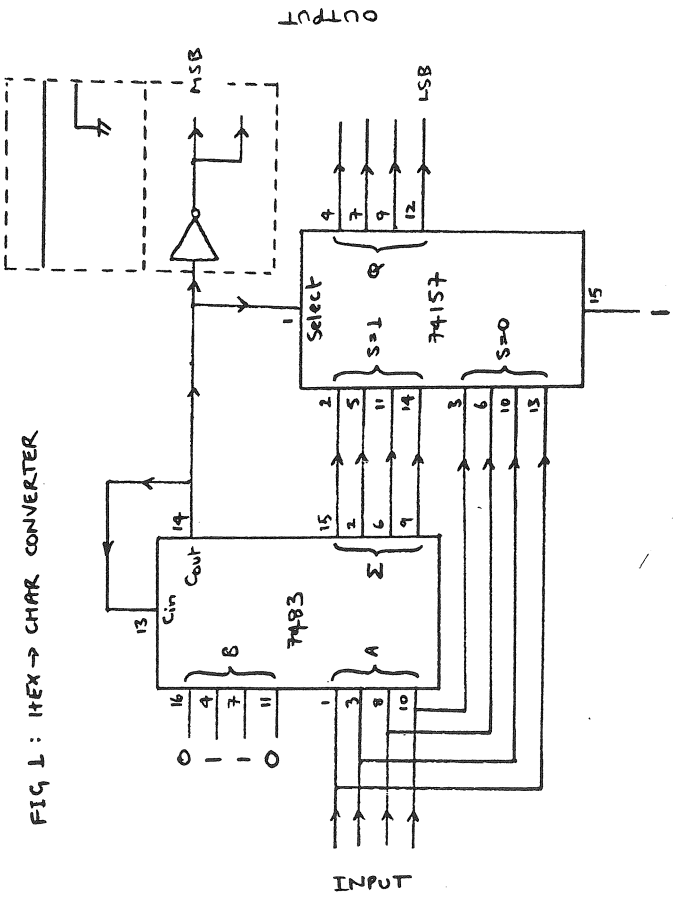


FIG 1 : HEX → CHAR CONVERTER

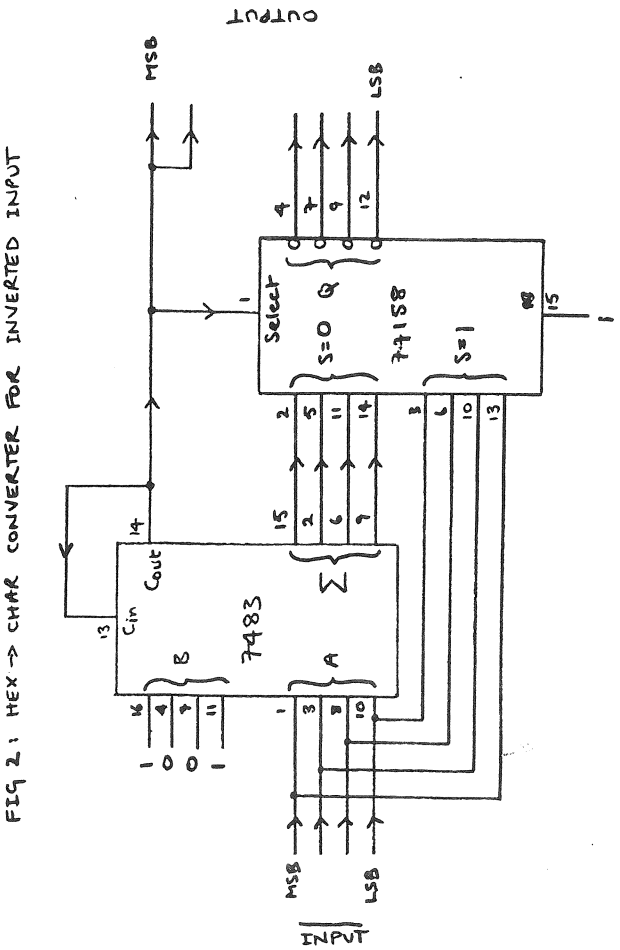


FIG 2 : HEX → CHAR CONVERTER FOR INVERTED INPUT

LOCAL GROUPS

MANCHESTER MEETS

Two meetings have been provisionally arranged;

One on Thursday 8th Sept, when we hope to have a talk on Terminal Interfacing.
The second on Thursday Oct 6th will be a demonstration by Limrose Electronics of their M6800 CPU board and 4k memory board.

The venue for these meetings will be the National Computing Centre, Oxford Rd.,Manchester at 6-30 for 7-00 (prompt) start.

As the venues/subjects are not completely finalised, could people check with D Wade (061 980 2755 home, 061 236 9432 ext 211 work) or Ken Horton (061 799 0192 home, 061 6333 ext 372 work).

MIDLANDS MEETING 26th JUNE

To start things off Alistair Nicoll showed us his Z80 system. His CPU board & memory board were built on standard Vero, double width DIP boards interwired with self-fluxing wire (as used on wiring pen systems). The CPU board has very few IC's & most of these are buffers, illustrating the low level of support needed for the Z80 chip. The memory board was based on 2102 type memories with octal buffers on the output. The boards were mounted on a mother board made up from standard 0.1" Veroboard interconnected with 64 way indirect connectors.

The front panel carried LED displays ahowing the data and address condition, a hex keypad made up from Greenweld type 'B' keyboards, and switches for Reset, Halt etc. As construction had only just been completed, no software was available, but he demonstrated several moves using front panel control. Altogether an excellent illustration that you do not have to buy fancy American kits to build up your own system.

Nick wright then showed us a beautifully made keyboard he had made using Greenweld type 'B' keyswitches. 4 type 'B' keyboards provide enough keys for one full ASCII keyboard with some left over for spares. The switches themselves have gold plated printed circuit type contacts, so are not recommended for heavy current. The keyboard was connected to an encoder made by John Diamond and based on the design in Vol 4 Iss 1 . This in turn fed an experimental VDU designed by John Diamond in which 20 IC's were breadboarded to give 4 lines of 8 characters on an oscilloscope. The circuit looked rather liike the picture on the cover of April's Byte.

Next meeting Sunday September 4th.
Roy Diamond 27 Loweswater Rd.,Coventry CV3 2HJ
tel; 0203 454061

LINLITHGOW LOCAL GROUP

On 24th July 5 ACC members met in Linlithgow to discuss forming a local computer hobbyist club. Three computers and solid software and hardware backgrounds were represented. It is hoped that we can generate enough interest from people in central Scotland to maintain regular meetings. Our next session is planned for 7th september at which time we hope to have a demonstration system present. Please contact Stewart Stevenson, Lindisfarne,New Well Wynd, Linlithgow, West Lothian (tel; Linlithgow 2657) for further information.

CHELTENHAM LOCAL GROUP

Future plans include an evening at the National Coal Board Research Establishment near Cheltenham to see how they use micros for instrumentation and control. We also hope to provide a workshop facility cum 'clubroom' at North Gloucestershire College of Technology on a regular basis.
M P Pullin 45 Merestones Drive, The Park, Cheltenham. tel; Cheltenham 25617

EDS BIT

Organisation of the ACC Convention - proposed in the last newsletter - has got off to a very slow start ('start' is an exaggeration !) due to the lack of;
a) A suitable venue in the greater London area.
b) Someone mad enough to organise it.
However, given some help (hint - hint) it is hoped that we can get moving and organise it for the end of '77 or early '78.

Following the 'Bus Special' issue, a lot of interest has been expressed in the Altair (S100) and SWTPC (S50) busses, so I'd like to organise a reference folder for each for the library. Would anyone with any information on either bus structure please send it to me for collation (the only item I've got so far is the 'Build Your Own Interface' article in Kilobaud No 6).

Talking about busses, I've been following the discussions about a proposed new ACC bus standard for some months now (in line with the ACCN editorial policy of publishing everything my maiden aunt thinks fit, regardless of my own views on the matter) and finally feel compelled to chip in and contribute my two-penn'orth;
-If you want an ideal standard bus then you will have to design it yourself, and so will everyone else.
-Otherwise accept whatever already exists (warts and all), which leaves us with;
a) The Altair/Imsai (S100) as the overwhelming favourite, heavily supported by many systems, although said by some to be technically nasty.
b) Possibly the SWTPC (S50) as there seem to be a lot of the SWTPC 6800 systems about in the UK.
c) Maybe Prof. J Nicoud's MUBUS, which is elegant and reasonably well accepted in European academic circles.

Finally, could I have all inputs for the next ACCN by October 8th at the latest please, I really must try to bring the publication date forward to at least the month shown on the front page !

LETTERS

PROCESSOR FOR SALE - BRIGHT LAD WANTED

I am fortunate to be the secretary of a small organisation and have seen the light as far as the benefits of a small micro are concerned for doing repetitive boring jobs in an office. Many of your correspondents seem to be either scientific or electronic wizards. How about some of us word processors having an inch or two ?

Our MP-68 arrived the other day and is being put together with 20k memory and the benefit of a FD-8 floppy disc which has a 315k capacity. I managed to get two terminals, one an Ultronic desk typewriter with punch and reader all set rather nicely in a neehole desk with two cupboards and a drawer or two from Chiltmead for £300. RS232 and ASCII coding electronics are your problem though Chiltmead are prepared to help. As the machine is an ordinary typewriter basically it has upper and lower case characters plus the normal bits and pieces and also has word and line editing facilities. The other unit we got is an Olivetti TC380 based on a TC349 which is a bank or stock control processor with miles of logic and a programming manual of its own. It has six print wheels giving upper and lower case and is based on the same principles of mechanics as the ASR33. Anybody interested in the latter as it is now surplus to our requirements should put in a bid over £200.

Is there a bright lad around who likes writing software ? I want to be able to have a 'renumbering system ' and a 'print using' facility in my 6800 system.

Colin Chatfield 25 Fore St.,Praze,Camborne, Cornwall tel; 0209 715901 Office hours.

SEVENOAKS & Co.

I would like to get in contact with anyone within 15 miles of Sevenoaks who has any kind of micro or mini computer system envisaged or running. I would also like to be able to help anyone who would like to form a two or three strong team to work on a micro system.
Martin T Robinson, Avenue Lodge, Seal Hollow Rd., Sevenoaks, Kent TN13 3SL tel; Sevenoaks 54309

IDEA APPEAL

Next year (77-78) is the third year of my university course, and part of my studies will be research (of some sort) and development for a project in the field of, or using, microprocessors. If I don't ask for a particular project of my own suggestion then I get allocated one. Unfortunately, at present I have no ideas that are feasible.

If you have an idea that you think will interest both me and my department, please send it to me - R Kirkby, 44 Whitby Rd.,Ruislip Manor,Middx.

A CROSS ASSEMBLER

I have a working FORTRAN cross-assembler for the Z80 on Imperial College's time sharing system (620 cards). If anyone is interested they can write to me for further information. Several changes are required to I/O to make it work on non-CDC machines, as the CDC 6400 has 60 bits = 10 characters per word. At least a SHIFT function is required. I am working on generating absolute load paper tapes for direct loading into my uP, and also on ASCII paper tape output for getting PROMS programmed (e.g. by Rapid Recall).
Hugh Comins, Silwood Park, Ascot, Berks.

CHESS & A GERMAN ACC

My video display and ASCII keyboard are now connected to my computer, it took 2 months to design and build the interface for them, however the interface does have a number of other features besides just driving the video and keyboard. It includes the interface for three cassette units which may be operated simultaneously, one cassette uses my high speed standard and the other two operate with the Digital Group standard, basically I am using the high speed cassette for program overlay and the other two for reading and writing data files. Also the interface handles the inputs from 3 sense switches for playing games etc. and an audio output which is just a single bit flip-flop which drives an amplifier and loudspeaker to generate tones, clicks and other interesting noises.

I also have 4 digital inputs which are available for things like frequency measurement, and a connection to my radio equipment permitting RTTY using my ASCII display and keyboard (callsign is DJOHF). The next hardware development is for analogue input and output, my old paper tape equipment is still connected though gets less use now, the printer is still usefull for hard copy and the paper tape for holding program master copies.

I know that some of the members have the KIM-1 and they might be interested in a full chess playing program which runs in the basic KIM-1 without additional memory, a cassette tape and full documentation is available from Robert M Tripp, PO Box 3, S.Chelmsford, Mass 01824 USA for $16.50 (world wide price).

There is also now a German ACCN and I wrote to them for details and they sent me the first copy of their magazine, they call themselves CCE (Computer Club Europe) and the magazine is a very glossy affair published in German and English called The Journal of Computer Encephalogia and Neurosis, however I have not decided whether to join or not as it costs DM85 per year (about £21) and the first issue was more than 95% copies of articles taken from various American publications, all of which I had read.For anyone with £21 to spare the address is CCE Postfach 11 08 68, D-6100 Darmstadt, W Germany.

Ian Spencer

SUMMER & SOFTWARE

Now that summer (British style) is with us the time for contemplating emulating a 1901T on your Weeny Bitter or possibly 4 dimensional StarTrek is with us. Being on holiday doesn't stop the Cybernuts! To help stimulate some ideas I will relate the current activities at Chez Nous.

The Digital VDU is finished (well actually there isn't a case on it but I'm sure not touching it again until winter) and I have written a VDU driver program for it. Also I have written carbon copies of Mikbug routijes and located the whole thing at the top of storage (20k now). My games are being patched to suit the new VDU program and Startrek is quite enjoyable now (on a TTY it is hell with short range scans taking forever). I also patched my 8k BASIC and the speed increase is fantastic. I put a copy of Life into it and thats quite entertaining (anybody tried Life in colour?).

This week I obtained my RT68, and before the people in the back row get too confused, RT68 is a MIKBUG replacemtnt ROM. It uses the full 1k though, unlike MIKBUG which only uses ½ of the ROM. The thing about RT68 is that it has improved commands including a dump command, and it will run 16 (yes, sixteen) jobs or programs together with 8 different priority levels. It works in priority or time slice mode and processes interrupts properly too. It has a timer location for computing times of jobs and there is a restart button that doesn't do a reset (it causes NMI instead).

The other thing about RT68 is that it can have any type of terminal (serial or parallel) on any port defined by a restart vector in storage. (Note the last point is for version 2 of RT68 only, version 1 can have an ACIA at alternative location 8014 only).

Using RT68, with its quite good manual, is really dreamy, you can fight Klingons, play Nim, service the central heating timer and still control your solar panels - storage permitting!

My latest aquisition is a cartridge drive for 3M data cartridge. You can store up to 2 megabytes per cartridge at 9600 baud data rates. Hopefully we will be able to have files and using relocatable programs I should be able, RT68 permitting, to run quite a good set up.

As a final comment, I have dissassembled my SWTPC 8k BASIC and am rewriting various portions of it so I would be pleased to talk to anyone doing similar things. I am now using a Co-resident assembler-editor and program development is considerably speeded up by this. I would strongly recommend its use by serious Cybernuts. Should anyone need any help, either hardware or software, with 6800 systems then I will help where possible and of course if you have MP6800 I can help you if you run into any serious snags (there are some bugs around).
D V Goadby 2 Lupin Close, Hinckley,Leics.

COULD Algol BE USED ??

With regard to my earlier letter about implementing binary scientific notation to decimal conversion, I stated that I thought that flowcharts were the only way of describing software principles without restrictions limiting use to a particular hardware architecture. I have since been thinking that perhaps something akin to Algol could be used.

e.g.

```
'BEGIN''COMMENT' THIS IS THE TITLE;
    FETCH(SX,MX,EX);
    FETCH(SY,MY,EY); (a procedure ?)
LABEL: SHIFTLEFTONEBIT(MX);
     EY:=EY+1
     'IF' EY=EX 'THEN' 'GOTO' LABEL;
    STORE(RESULT)
'END' OF RUBBISH EXAMPLE;

'PROCEDURE' FETCH(X,Y,Z);
'COMMENT' GETS REQUIRED NUMBER FROM "SOMEWHERE"!
          RETURNS NUMBER IN THE FORM "SIGN,MANT-
          ISSA,EXPONENT";
etc.
```

S G Bailey

MONITOR

I saw a letter in the latest ACCN re TV monitors and I have some news that may help members.

Wire frame monitors (without case & PSU) TTL video & synch (you provide 12V DC @1A stabilised)

9" monochrome £126 1 off
12" " £128

Boxed with mains derived PSU, composite video

9" monochrome £180
12" " £200

Available from Digivision Ltd.,9 Claymill Rd., Leicester.

M H Baker

*** Had a note from Crofton Electronics Ltd., 35 Grosvenor Rd.,Twickenham,Middx. 01 891 1923 saying that they can supply secondhand monitors, serviceable £45, rebuilt £70 *** ed

PDP8 & EDUC-8

I have a PDP8/L running on BASIC & FOCAL - anyone in High Wycombe area who is interested is welcome to come and use it for their own programs, at weekends, please phone first. I am mainly interested in the Hardware side, and would welcome any advice from experienced programmers.

Two years ago, Electronics Australia published a series of articles covering the design of an all-TTL computer, called the EDUC-8. Although rather limited in capability, it is a very good educational machine, built entirely of common TTL IC's on 5 boards. In its basic version it uses 2 Fairchild 93415 1024 bit RAMs giving 256 words of memory, but this can be expanded. Anyone interested, I have the machine I built still working, and the manual.

Nigel Dunn 21 Campion Rd, Widmer End,High Wycombe tel (weekends only) 049 47 4483

IDEAS FOR SPENDING YOUR HARD-EARNED CASH

TINY BASIC (Tom Pitman's) runs in 2k+ and is written for 6800 or 6502. There are a host of versions - simplest is to send a description of your system and $7 to Itty Bitty Computers, PO Box 23189, San Jose, Ca 95153 and you'll get by airmail a full description plus a paper tape for the version most suitable. They also have an 'experimenters Kit' which shows how to expand Tiny for $12.

MICROCHESS is designed to run on a basic KIM-1 (with only 1.1k of memory !) and while not playing an expert game can certainly give practice on the five openings provided, and provide a good game for ordinary mortals. Three depths of play are possible (taking 3 to 100 seconds). $16.50 buys you the manual, program listing, cassette tape and airmail from The Computerist, PO Box 3, S.Chelmsford, MA 01824

Also from The Computerist, their PLEASE package enables games like a reaction timer, clock, shooting stars, mastermind, and arithmetic routines to run on a KIM-1. Airmail, manuals & cassette tape comes to $11.

While talking about KIM-1, Eric C Rehnke of PO Box 33077 North Royalton, Ohio 44133 edits the KIM-1/6502 User Notes. An absolute mine of information ! Nos 1-6 (back issues) come to $8, while a subscription to Nos 7-12 costs $10 (airmail).

The Computer Education Group produces a magazine for anyone interested in the teaching of computing in schools or colleges, also conferences. A year's sub costs £2 from Mrs P Jackson (Treasurer) of

North Staffordshire Polytechnic Computer Centre, Blackheath Lane, Stafford.

Very Highly Recommended. 'The Best of Byte' and 'The Best of Creative Computing Vols 1 & 2'. Check latest prices in Byte! It's easiest to order them on Access/Mastercharge card.

Dennis Holman

DIP TIP

I have just discovered the Vero DIP breadboard (No 06-0166 F) It is the solution to my homebrew problems. A perhaps unusual method of use is;

1) Solder Soldercon pins as sockets for all IC's to the plated side of the PCB.
2) Make as many wire jumper connections on the component side as you like without obstructing IC's.

The 42 pin edge connector makes an excellent bus structure (perhaps a standard for the ACC). Cost is very low when compared to the other method; wire wrap.

Ken Talbot

BUSTALK 1; VIVE LE S100

The only bus that even approaches being an industry standard is the S100. Even with its 'shortcomings' (IF they exist; I'm not aware of any) it is the most flexible and the most affordable, and the S100 is increasing its hold on the market daily as more and more cheaper and cheaper S100 peripherals become available. Certainly the most cost effective way of getting started would be;

Godbout motherboard with edge conn		$80
Morrow's 8080 MPU board		$250
Godbout 8k RAM board		$164
	Subtotal	494
20% ;P&P,duty,VAT		100
		$ 594
@ £1.o = $1.7		£ 350

This of course includes the I/O device on the CPU board (hex keyboard & 7 segment).

Just to provide a benchmark, for publication any new 'standard' should also include the source and or pricing of an 8k RAM board. (for comparison, S100 £115).

The edge connector contacts are 0.125" centre to centre (not 0.156" as stated by Tony West). Edge connectors are cheap and easily obtained from the States. Prototyping boards are also available (The Club could really help here by encouraging a UK source, could we beat the US cost of £17 ?)

I have the MOSTEK F8 evaluation kit operating on the S100 bus now with 9k of RAM. On hand are the SD Sales Z80 and TDL's monitor board which I should have operating any day now. A 'cheap' VDU is on the workbench (not operating yet).

One commercial announcement. From my experiences one should have no fear of dealing with Godbout Electronics (see adverts in Byte for large range of microprocessor products). To date Godbout has;

- Shipped an order that I had underpaid and sent me an invoice (how many UK firms would have held the order ?)
- Sent me £15 worth of parts free to assist to trouble shoot a minor fault on a RAM board.
- Answered all queries within a few days and by air mail.

In addition, it typically takes three weeks from the day I mail an order until I receive the goods, and this includes allowing personal cheques to clear. Again, how many UK stockists can beat that ?

One word on duty - if the word 'computer' appears in the customs declaration the normal duty and VAT charge is 17½%. So take the dollar price, add $5 to $10 for airmail postage (which you will need to specify), multiply by 1.175 and divide by 1.70 to find out what it will cost you.

Len Talbot

THIS IS BUSTALK 2

The last ACC newsletter (June) contained no less than three articles discussing standard busses. This is very commendable, I believe the subject to be most urgent. A bus structure which will support most current & future micros is highly desirable rather than the S100 bus which is only intended for the 8080 family.

As always, there are snags with getting people to agree, especially if they have already started their own projects, but unless agreement is reached fairly quickly, say early '78 at the latest, I think that the S100 bus would become standard here. We NEED a standard bus quickly to keep the S100 bus out and also to give prospective European hobby market manufacturers firm ground on which to market their equipment.

My own thoughts mostly agree with Messrs Pat Crowe & Dave Howland;

1) I agree that double Eurocard is the 'best' format for card size.
2) I agree with a two part connector and 64 way seems reasonable.
3) I agree with most of the named signals, but disagree with some signal levels. I would prefer to see all control type signals as asserted low, but address and data lines should be active high, this is because some chips, mostly bipolar, are quite capable of driving the bus direct but would need a number of extra chips purely to invert levels.
4) The drive levels to the bus quoted at 45mA and 50pF seem unnecessarily high. I believe this is the sort of level that DEC & Data General specify for their open collector busses and requires slightly special chips.
   Messrs P Crowe & D Howland do not state whether tri-state or open collector should be used for data & address busses. I would prefer data and address busses to be defined as; tri-state, active high, capable of driving say 32mA @50pF If the input to each card for all bussed signals i.e. data, address and memory/peripheral control signals, is defined as one TTL load, this allows 20 cards !! to be driven without having expensive driver chips.
5) To have truly future use as a standard the data bus should be 16 bits wide. There may be only some four 16 bit micros now, but we can be sure that more are coming and we'll all want to use them won't we ! It would help if it could be 'slotted in' and anyhow, how about dual 8 bit micro systems ? Space can be made by moving, say, IUD3/4 and OUD2-7 to the second connector. That's what its there for anyway isn't it ?
6) I agree with Tony West that the power pins should be distributed according to loading, but in order not to increase the number of pins required I would arrange them as follows;
   4 pins for +5V 4 pins for 0V
   2 pins for +12V
   1 pin each for -12V & -5V
   and forget about PUD.
   Tony's point about on or off card regulation is difficult, both ways have merits. After some thought I have decided that off card regulation is preferable. Among other reasons it allows a separate decision to be made on the power supply i.e a small system running from mains would probably use linear regulation, a larger system might tend to use switching regulators, but if either version were battery (car ?) powered it would use switching regulators to improve the efficiency. On card is invariably linear hence no choice is available.
7) I disagree with Tony West's thought that the bus should only be for memories. While many of us are only just getting our systems together, and memories may seem of great importance, we can expect a time in the not so distant future when some of those peripherals we would all like will get to a price we can afford. Like floppy discs and decent printers etc. IO will be just as important than and if a standard bus can be agreed now there will be less problems in the future.
8) Tony's thought of having an ACC standard memory card is a good one but a 'standard' memory card cannot be produced until there is a standard buss and there are other problems. Should it be static or dynamic ? if dynamic should it have on-card or off-card refresh ? How much memory should the card hold; 4k x 8 bits, 8k ? 16k ? Should it be possible to determine the address in small subsections, say 1k ? I think this raises a whole new issue that should wait until a standard buss has been determined. At the recent inagural meeting of the North West Group memories took up a large slice of the discussion. The only point worth mentioning seems to be that to allow for later 16 bit data working, any 'standard' card should have a means or selecting whether it is data bits D0-D7 or D8-D15. This allows two 'standard' cards of 8 bits to be paralleled for 16 bit data use.
9) As P Crowe & D Howland seem well advanced on a buss specification, it would be nice if they could produce a complete preliminary specification showing signals, allocated pins, voltage levels and timing diagrams. We would then be on the way to at least an ACC standard bus allowing members to borrow from each other and/or produce temporary large systems for use at exhibitions.

R A Munt

RT68 THE SHAPE OF THINGS TO COME ?

Earlier this year a small advert appeared in Byte, it was for RT68 and it described what seemed to be an offer you can't refuse. I sent off my order and recently received my own RT68.

RT68 is a MIKBUG replacement, it is plug compatible with it, also it uses all 1k of the ROM. In essence it has 2 modes of operation. Firstly it will act like its predecessor with all of the standard MIKBUG routines, except the commands are not all the same. These commands are;

```
G             Go to program
R             Print registers
L             Load tape
P aaaa,bbbb   Punch tape
D aaaa,bbbb   Formatted dump (very useful)
B aaaa        Set breakpoint at aaaa
M aaaa        Memory examine/change
      aaaa = start address for P & D
      bbbb = end address    "  "  "  "
Three additional commands are
S             Activate multitask operating system
(ESC)         User defined function, program resides
              an Hex 7000 (user written)
E aaaa        Execute task at aaaa
```

Also there are 7 error messages showing what went wrong. The breakpoint command stores the old opcode it removed from aaaa and after a breakpoint, typing G (Go) restores the code before running.

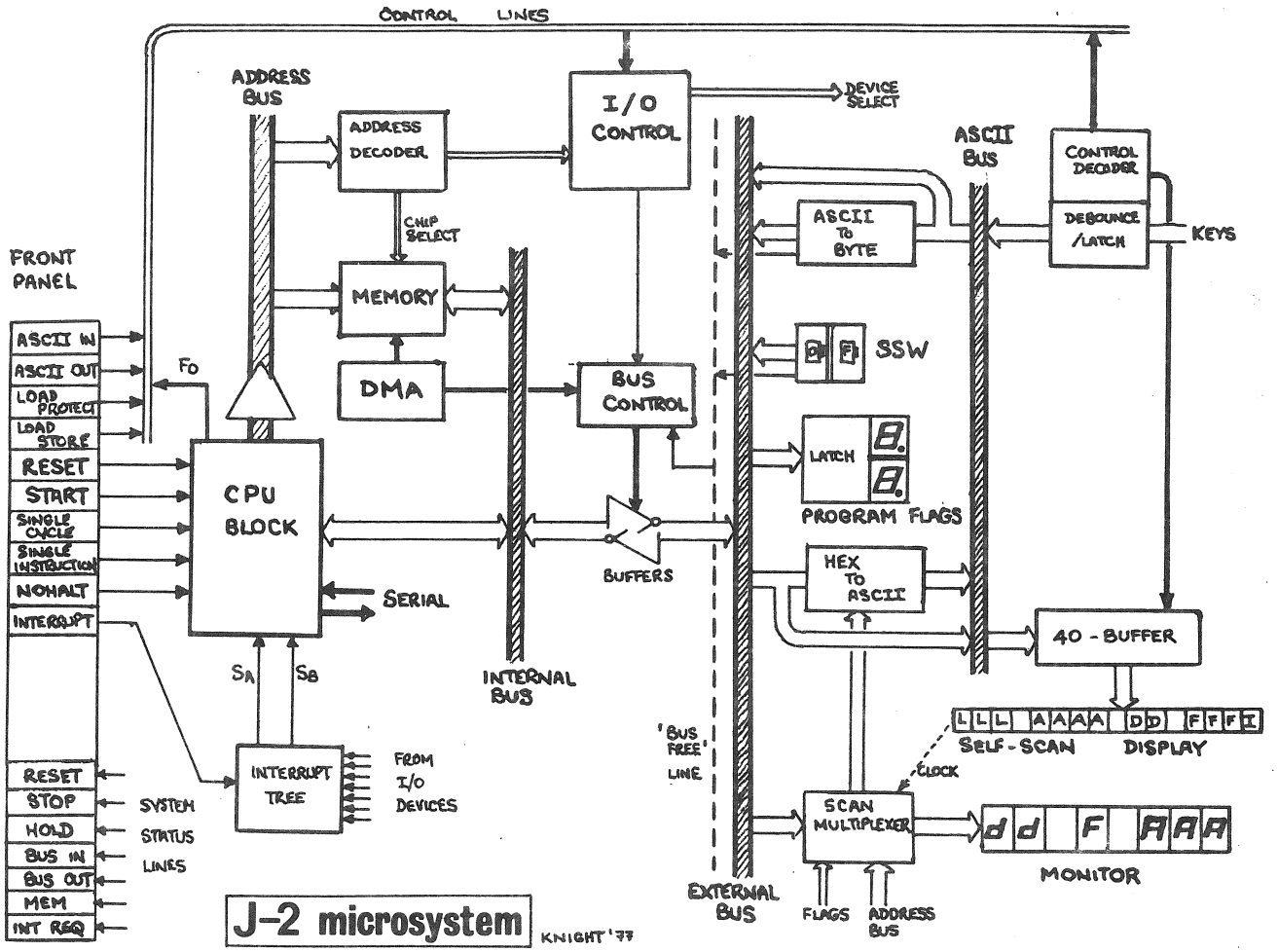
In multitask mode (type in S) there are other things that come into play. There is an abort switch that causes an interrupt on the control port without resetting the PIA's etc. There is a timer input which gives interrupts (ticks) every 1/50 sec ,or using another oscillator instead of 50Hz mains you can use anything between 10 and 100 Hz. There is a timer location that is updated at each tick. At each interrupt there is the possibility of task switching if a task has run for its alloted time slice. Essentailly there are 16 tasks with 8 priority levels that can be in the processor at any time. There is a task status byte for each task. It contains task priority (0-7), time limit (1-15 ticks or 0 is unlimited) and a flag showing the state of the task; active or inactive. Task switching occurs at interrupts or by the tasks enabling and disabling other tasks using subroutines within RT68.

There is a superb programming book with the ROM and indications of special programs being written to use RT68 to the full.

RT68 version 2 will have the capability of using any interface (ACIA or PIA) at any location by using a vector in storage to indicate location of the I/O. This will allow a very versatile structure and simplified I/O handling.

RT68 is available in this country from Haywood Electronic Associates, 11 Station Approach, Northwood, Middx HA6 2XN and is about £40. Meanwhile I am having some very interesting ideas on using my RT68, with the only limits being my imagination ! It is available direct from the USA for $40 + $5 handling from Microware Systems Corp., PO Box 954, Des Moines, Iowa 50304.

D Goadby



The recent issues of ACCN seem to be getting more and more lively - perhaps it will one day go glossy (and pricey) as a sort of British Byte ? But instead of writing about all the interesting sidetracks which come to mind, I'll stick to the main one; SC/MP

Firstly; I'd like to form a SC/MP or 'small mpu' group, if nobody else has suggested it. This would be to cover the interests of people with limited budgets or experience, but also to promote the use of such microprocessors for simple dedicated applications, including a clever I/O for a main device like the Z80. It could take in other processors like the 4004 (now promoted by Practical Electronics)

Secondly; A few things about Mr Marshall's otherwise nifty design bothered me. If I read his circuit diagrams correctly, he has decoded the lowest 12 bits (A0 - A11) to define his page, and then used the strobed data bus (DB0-DB3, equal to A12-A15 at NADS time) to define the block within the page. This is contrary to normal practice, especially as the strobed bits can be omitted if you don't need more than 4k of memory (and many SC/MP rigs don't) and must make normal relative addressing impossible. Also, to save decoding the chip enables with X16 and X17, why not base the system on blocks of 256 bytes directly, which saves using indexed addressing all the time. Since a block of 1k requires 10 bits to decode, but since A8-A11 have also been allocated to the page decode, it appears that A8 & A9 overlap, otherwise he's got 16k into 4k space ! I also noted, as with other designs, practically no provision for IO, and no advantage taken of the serial and flag bit IO which SC/MP offers. However, this is not meant to be serious criticism, and it was good to see that somebody had made the effort to go beyond SCRUMPI.

Lastly; into the firing line myself with a description of my development system, J-2. This is very much a hardware oriented system, designed to be very versatile, and to accept almost any MPU or I/O device, and the emphasis is on the I/O; in this respect it should not be considered of home computers. A full circuit diagram is not practical, there are 83 chips at present, including a SC/MP, but the block diagram shows the main points. The PROM and Z80 CPU which are being added are not shown. The principle input device is a commercial keyboard which also has a number of hardware programmed special function keys, like a big calculator, there is also a pair of Hex thumbwheel switches and single bit switches for SA and SB, and tape recorder (CUTS) serial or byte input. Other things are planned. The principal output device is a 16 character Burroughs Self-Scan, but a calculator display is used to monitor the data and address busses, and breakpoint codes or diagnostic symbols can be displayed on a pair of seven segment indicators or on four Burroughs 15 segment Giant Nixies. Serial output to a tape recorder is either CUTS by software, CUTS by a VCO controlled with a single bit, or direct bit stream as described in an issue of Byte. One of the input devices can be designated the IPL (Initial Program Load) device by a switch; should the keyboard be faulty, it can be unplugged and programming done from the thumbwheel switches (not as tough as bit-switches, but mearly !). Otherwise, complete bytes are assembled by pairs of keystrokes under hardware control. Likewise the SSD can be removed and the system will still give the essential information for stepping a program on the calculator display. In other words, there is a high degree of redundancy, and no assumed dependance on a ROM monitor, although one will be programmed in the future. The present System Monitor resides in the low area of page 0, with the top end allocated to I/O, addresses OFFF to OFE8 at present, which represent not 24 devices but 24 overall mode selections. Page 1 is dedicated to 4k static RAM. Software control of I/O mode will of course be used since that is the object of replacing logic with an MPU, but the hardware system also provides it. For example, the SSD normally runs in a 'monitor' mode, in which it displays (during CPU HALT state) address (4 x hex) , data (2 x hex), 3 flags and Interrupt, and Program Counter (3 x BCD). When working as a program output device it can be used for an ASCII string (for example short assembler statements or messages), or ASCII with special 'home-made' characters inserted, or full graphic (110 x 7 dot matrix). A shift register buffer, 40 ASCII characters using a 2519, is also provided for text handling. This

overcomes many of the disadvantages of having no Teletype, and in fact the keyboard can communicate directly with the SSD and the tape recorder without reference to the CPU at all for handling unformatted ASCII text.

Programming from the keyboard allows the following modes; direct keystroke (for 12 instructions only), byte-opcode, and direct ASCII data. The system can be made to load-and-execute-memory (SCRUMPI type), load and execute with memory locked out (for branching in and out), execute branch/step sequence (Altair type), or else load by true DMA (processor disabled). There is a polled interrupt system, with SB and FO used for synchronisation/handshake where necessary.

The keyboard is part of a VDU, which latter will be used for graphics only, either raster-scan or vector. I am looking for a small X-Y plotting table.

One final note; the clock on my SC/MP ran at almost exactly 1MHz with 390pF across the timing pins, rather than 500pF as you might expect. Using a driven clock from a J-K divider, 2.5MHz was obtained with reliable operation of a simple loop program for over 15 mins. (I didn't test for longer). The entire system consumes a modest 2.3A (5V) and 250mA (-12V) excluding the 12V indicator lamps.

J R Knight.

D·I·Y COMP CONF

The packed lecture hall at the 'Build Your Own Computer' conference on May 14th showed that amateur computing has well and truly arrived in this country. Over six hundred people had paid good money to spend a glorious Saturday inside the IEE at Savoy Hill, myself included. What did we learn ?

Microprocessor based computers dominated the meeting, though 'Byte owner, Manfred Peschke, told that up to 25% of his readers who have computers, had home-brewed (non microprocessor) machines. The only place where such machines were to be seen here were on ACC's stand in the exhibition, where a WB-1 was on show (Tony Cassera's - ed)and also photos of the Galdor Centre's ICL machine to remind people that if keen enough you can own a big main-frame machine. Also on our stand was the new 7768 machine described in the April newsletter. Among the micros the Z80 seemed to be the in thing, though actual hardware shown or described in detail was 8080 or 6800 based. Guy Kewney of 'Electronics Weekly' had some interesting comments on micro-kits. He issued the dictum that 'Mk 1 of any development board won't work' and found heartfelt agreement. He also reminded us that many kits are designed to stop you extending memory space, manufacturers not wishing to undersell their own one-board computers. Several speakers reminded us of the tedium of working in machine code; the general feeling being 'go all out for a keyboard and some form of assembler'. Actual software for micros is now very cheap in the States but little seems available yet in the UK. A figure of $25 was quoted for a BASIC software kit. TINY BASIC got several mentions. It is available in the Intel software library and needs only 4k of memory. BASIC as a language dominated the meeting, others receiving little mention.

So you go for a BASIC package. How do you get it into your computer's memory? Cassette based systems using the Kansas City standard code are the commonest way of conveying programs. The magazine 'Interface Age' has given away a flexible LP record containing a 6800 BASIC assembler in a recent issue encoded in this format. Papertape is still with us. There are very simple readers in which you pull the tape through by hand. Your Anglepoise is the light source, there is simply a row of photodiodes below the tape. Presumably the strobe is generated from the sprocket hole. New to me was bar-coded software. Peschke showed a booklet printed with bar code, another BASIC assembler. FORTRAN to follow. Price about $7.The code is read in by a hand-held wand. This seems the untimate in cheap portable software. Has anyone details of construction of these read-wands ?. All this software needs memory space, prices of memory will get cheaper and Robin Woods of Texas showed a 80k bubble memory in an inch-square chip that will soon be available.

What do you do with all this kit ? Richard Monkhouse showed colour slides from his video synthesiser which were quite remarkable. They were produced by feedback of a colour TV camera looking at a colour TV. Several examples of music and voice created by amateur systems were played to us, demonstrating another line of interest. We saw some slides of a typical amateur's den in the States; Tektronic scope, Altair system, and all making us rather envious.

Software experts J L Page and the famous R H Uiterwick outlined how you go about writing an assembler, analysing character strings to decipher commands. Software development is a major interest in the USA hobby scene.

The conference's organisers 'On-Line Conferences' promise another meeting next year and I hope they can keep their word. Certainly they deserve another successful meeting. Maybe the time is not far off when we will have something to rival the big States jamborees like the San Fransisco West Coast Computer Fair.

Anthony Cassera

~~SIMPLE~~ SC/MP'R

SUPER SCAMP DEVELOPMENTS Bill Marshall

New improvements on my SC/MP system described in the June newsletter may be of interest. The panel buffer board has been completely rebuilt, with the addition of a full DMA facility, and a READ button added to the front panel. The memory is directly accessed in the periods between machine cycles when BREQ is low. This means that the DMA does not involve cycle-stealing, and thus in no way interrupts program execution.

In order to read from anywhere in store while a program is running the appropriate address is set up on the address keys, and the READ button pressed. Reading is continuous all the while the button is held in, the latches holding when the button is released. The address keys can be changed while the button is held in, to read from another location.

In the previous design the store could be accessed directly with the processor in Reset. This has been extended so that address keys and data LEDs are switched onto the bus automatically when the processor enters a Halt state as well.

In a similar way the WRITE button can be used to place data into store from the data keys between cycles and when the processor is halted. In my case, I have found that when using the former mode the Write signal to the RAMs is delayed sufficiently relative to the RAM address stabilising to ensure that data is written only into the desired location. However, experiments with various RAM chips have shown that corruption of other locations may sometimes occur. Using faster chips seems to cure this, but I am not too bothered as the original idea was only to be able to write into store when the processor is halted. The DAM read however has no such problems and is proving very useful.

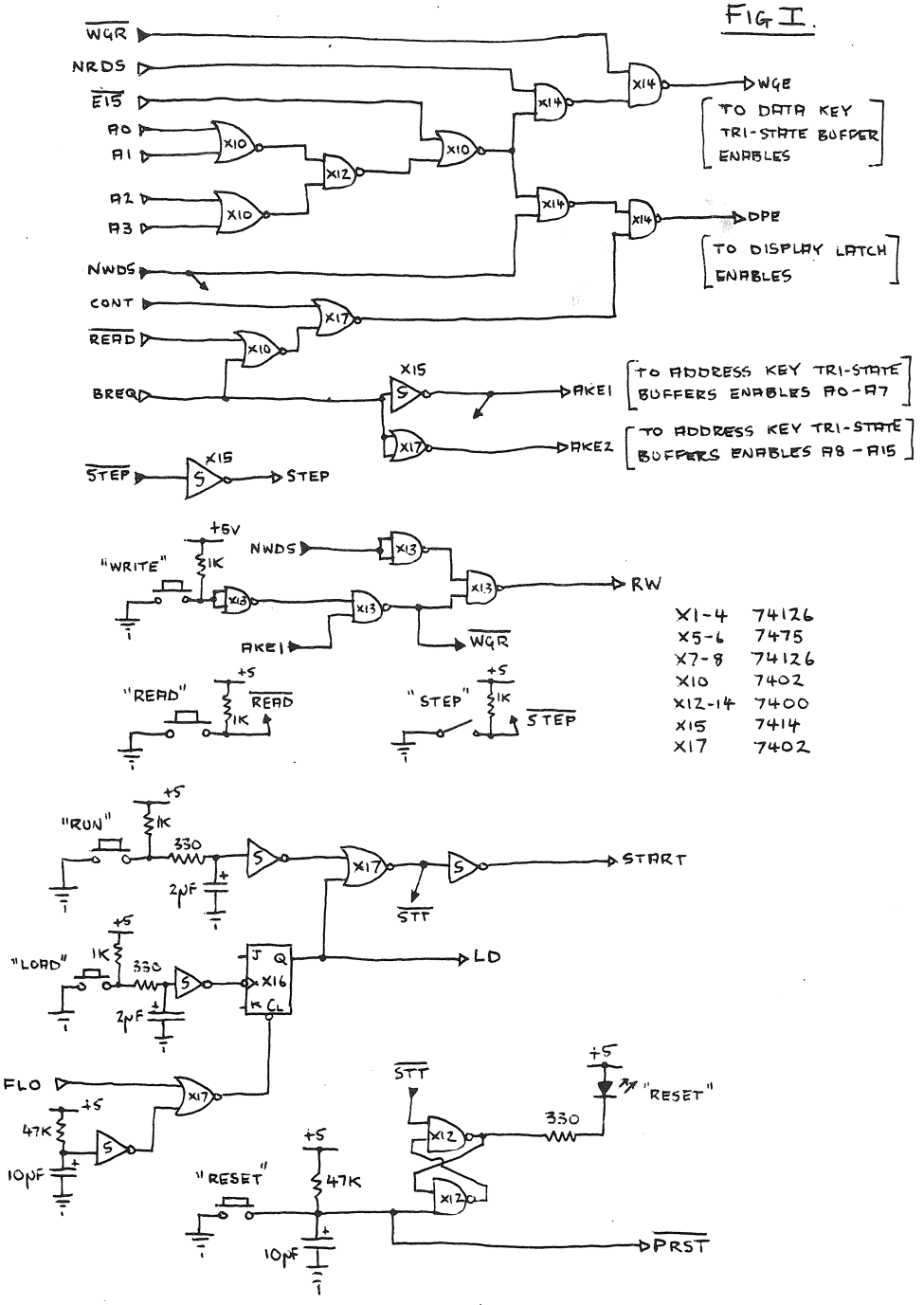
New Peripheral Addressing

Panel LEDs and data swithes now have the same address; FXX0, selection being performed by the read & write strobes NRDS & NWDS.

The paper tape reader has address FXX1. Apart from the keyboard and VDU, subsequent peripherals will have addresses FXX2, FXX3 etc. This helps to relieve the problem of a lack of direct addressing in the SC/MP. Pointer register P1 say, is set to FX00 and then subsequent load and store instructions involving P1 can select the appropriate peripheral using the displacement byte. Note that as the peripherals look like ordinary store to the SC/MP,

PANEL BUFFER BOARD MK. II

FIG I.



such operations as Exclusive ORing the accumulator with the next paper tape character are possible with one instruction.

Paper Tape Reader Interface & Bootstrap Loader

The paper tape reader I am using is the GE PTR 661A, obtained last year through the newsletter. RDTG goes to the trigger input, the diode clamping the signal to just above ground. The monostable triggering gives a -5V edge, sufficient to trigger the reader. The monostable period is set so that the SC/MP is held up while the tape is moving, by pulling down NHOLD. The resistors on the data and sprocket inputs are level shifting components.

Also on this board I have put a 1702A E-PROM containing a basic binary loader program. This PROM is treated as part of the main store and contains locations EX00-EXFF. On pressing and releasing the LOAD button the X16 flip-flop (Fig 1) flips over and sets LD high starting the SC/MP. This LD signal inhibits the memory page decoder 74154 and enables the PROM. This results in the SC/MP 'thinking' that it is pulling its first instruction from 0001, whereas it really takes it from E001. The first instructions in the PROM set the program counter to the PROM address and then pulse the flag output FLO, resetting the flip-flop X16. The bootstrap loader now continues under normal SC/MP control. The listing for the loader is given below and it offers the following facilities;

It ignores leading blank tape.

It will load any length tape up to 64k characters.

It will begin loadinh at any desired point in the 64k field.

It will auto start the program at any point in the 64k field.

Listing for Basic Binary Loader

```
C4 E0   LDI E0    ;load program counter with PROM
34      XPAH (P0); address
C4 01   LDI 01
07      CAS       ; set FLO high
C4 00   LDI 00
07      CAS       ;set FLO low
C4 F0   LDI F0
35      XPAH (P1);load P1 with peripheral address
C1 01   LD 1(P1) ;input from PTR
98 FC   JZ -4(P0);ignore leading blanks
32      XPAL (P2)
C1 01   LD 1(P1) ;1st two char on tape give tape
36      XPAH (P2); length to P2
C1 01   LD 1(P1)
33      XPAL (P3);2nd two char on tape give start
C1 01   LD 1(P1) ; address for loading to P3
37      XPAH (P3)
32      XPAL (P2)
98 09   JZ +9(P0)
32      XPAL (P2)
C1 01   LD 1(P1) ;input data char from PTR
CF 01   ST @1(P3);store char & inc address counter
                 ; P3
C6 FF   LD @-1(P2);decrement tape length counter P2
90 F4   JMP -C(P0)
32      XPAL (P2)
36      XPAH (P2)
98 03   JZ 3(P0)
36      XPAH (P2)
90 F1   JMP -F(P0)
36      XPAH (P2)
C1 01   LD 1(P1) ;load low byte of auto-start addr
33      XPAL (P3); from tape
C1 01   LD 1(P1) ;load high byte of auto-start
37      XPAH (P3); address from tape.
3F      XPPC (P3);transfer control to auto-start
                 ; address.
```

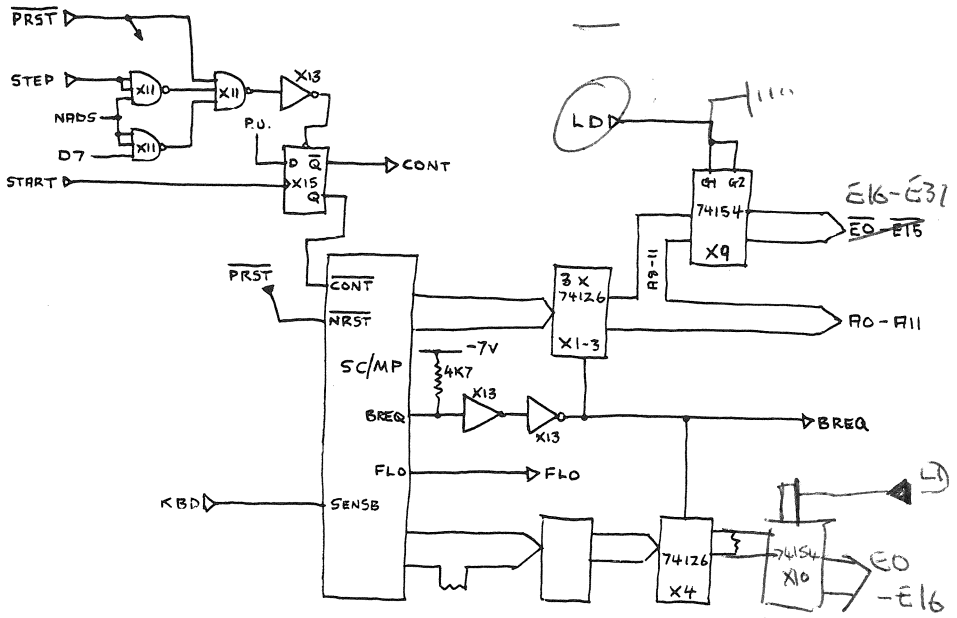
Keyboard Interface

I have just purchased a Clare-Pendar keyboard and include the diagram for the interface. The KBD signal goes to the SENSB input of the SC/MP and is monitored by the handler routine when a key is pressed. When a 'key pressed' indication is given the SC/MP accepts data from address D4XX. Addressing the interface clears down the 'key pressed' flip-flop X1.

Conclusion

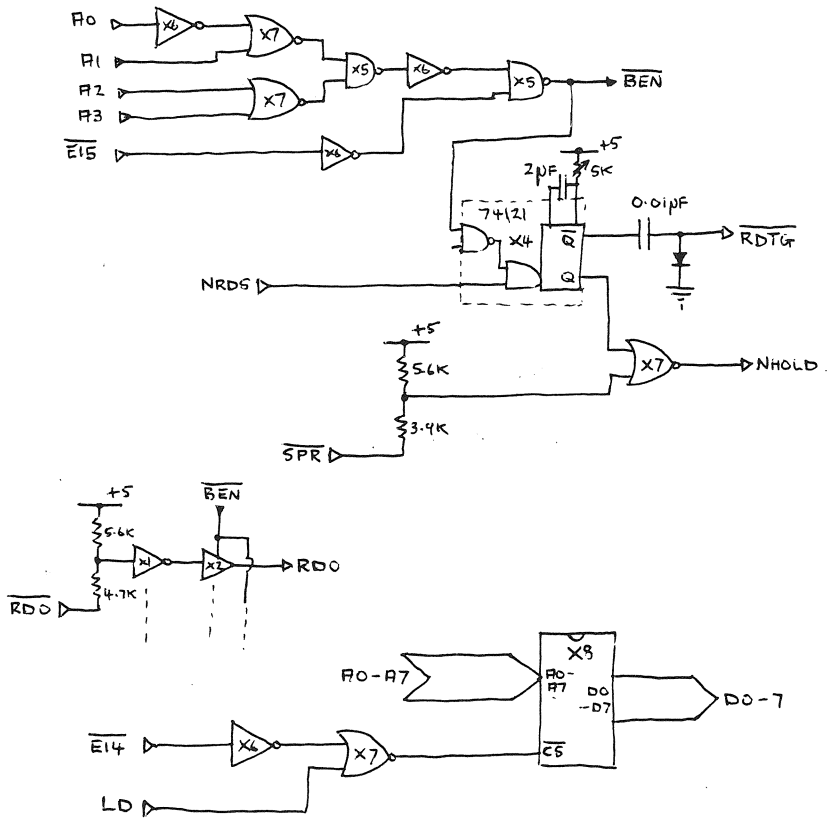
My next project is a VDU, the design of which is almost complete, using ideas from a variety of sources. The VDU store will be regarded as part of the main store by the SC/MP, and all cursor controls etc. will be implemented by software.

After all this hardware construction I hope to get on and write some software! A mini operating system with a simple assembler are on the agenda, and should give a useful working computer to play with.



CHANGES TO THE MICROPROCESSOR BOARD. THE REST OF THE CIRCUIT AS DESCRIBED IN THE JUNE 1977 NEWSLETTER REMAINS UNCHANGED.

FIG II

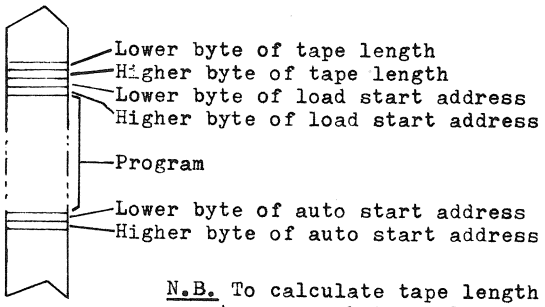


X1 7404
X2-3 74125
X4 74121
X5 7400
X6 7404
X7 7402
X8 1702A

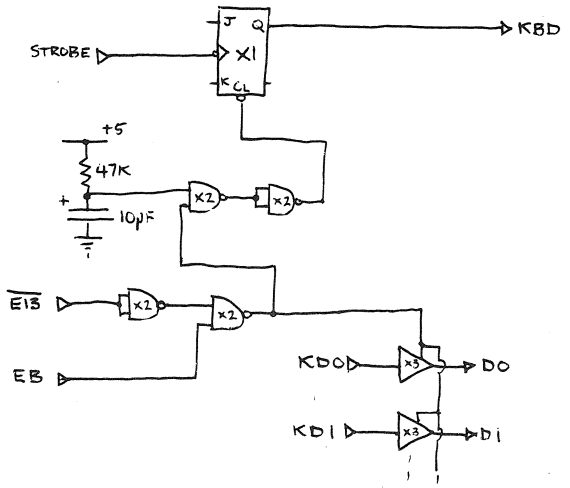
PAPER TAPE READER BOARD

FIG III

Basic Binary Loader Tape Format



N.B. To calculate tape length count program bytes only.



KEYBOARD INTERFACE (CLARE-PENDAR KB6)

X1 7476
X2 7400
X3-4 74125

FIG IV

BOOT YOUR OS

BOOTSTRAP LOADING OF OPERATING SYSTEMS FROM CASSETTE TAPE. Guy Burkill

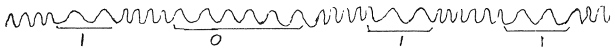
Most MPU systems benefit enormously from the use of some kind of operating system. My own processor uses a calculator keyboard and seven-segment display for input and output, and these are driven from software in order to reduce hardware cost. Logically, one would want to store the software on a PROM. I have not done this because;

a) PROMs are expensive.
b) They tend to require 3 different supply lines, power supplies are expensive.
c) The software is continuously under development, and EPROMS are at present difficult to reprogram.

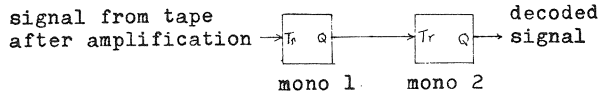
Therefore I store the system monitor on cassette tape and reload it each time I power up. The slight nuisance - loading takes about 10 seconds - is easily outweighed by advantages of economy and the versatility of the system.

My processor is a MOS Technology 6502, but there is no reason why the technique now described cannot be slightly modified to suit any other processor currently available.

The tape format is as follows; most of the cassette is recorded with a continuous 2400Hz signal. Interspersed with this are pulses at 1200Hz. A pulse of 2 cycles at 1200Hz represents a '1' bit, a pulse of 6 cycles of 1200Hz represents a '0' bit. (Note that the frequencies are compatible with the CUTS standard so that the hardware may also be made use of in decoding tapes recorded with this format). Thus a typical signal from the tape might appear as;



We require to decode this signal in such a way , initially, that we obtain a high output for the 2400Hz tone and a low output for the 1200Hz tone. A suitable circuit can be obtained by using two consecutive monostables thus;

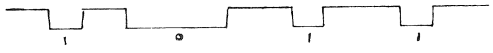


The monostables must be the retriggerable type - a 74123 package contains 2 of them. 74121's will not work.

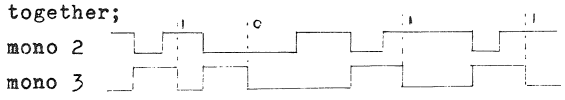
Mono 1 has a period of about 0.6mS. If a 2400Hz tone is applied the monostable will be continually retriggered, and it will produce a constant high output. But if a 1200Hz signal is applied, mono 1 will time out between cycles and will produce a train of negative going pulses at 1200Hz.

The output from mono 1 is now fed to mono 2.This has a period of about 1 mS. Now if we feed a continually high signal to it, it won't be triggered and the output will remain low. But if it receives a train of pulses at 1200 Hz, it will be retriggered indefinitely, and the output will go high.

Inverting the output of mono 2 now gives the decoded signal which was specified above. Let us look once again at the sample waveform above, this time as it appears after passing through our two mono's;



One more monostable, which this time may be a 74121, completes the signal processing hardware. It has a period of about 3 mS, and is triggered by the negative-going edges of the above signal. It has the property that it will time out before our '0' pulse has ended, but after the '1' pulse has come and gone. Call this last monostable mono 3, and let us look at the outputs of monos 2 & 3 together;



All the processor has to do now is to wait for the negative edge of mono 3, and then sample the output of mono 2 to determine whether the bit was a zero or a one. We can attach the two monostables to two pins of a PIA, and then a 32 x 8 PROM will provide sufficient space for us to package up the incoming bits in bytes of 8 and neatly stack tham into successive RAM memory locations, by using some software to simulate those much more expensive UART's. In fact, with a little cunning I was able to do this using a 16 byte diode matrix, but was then restricted to a 256 word operating system. By using a 32 byte PROM I can now load any size OS at a speed of about 30 bytes per second.

I arrange the PROM so that in 'load' mode, it responds to any address on page FF; RAM memory in that space is made write-only so that no bus conflicts occur. In 'run' mode the PROM is disables and RAM functions normally as read/write; the operating system that has been loaded in may now be run.

Software for the 6502 is as follows;

Tie monostable 3 output to S.O pin (sets V flag). Monostable 2 is on pin 7 (most significant bit) of a PIA responding to address 0230.

```
FFDE A0 00     BEGIN:    LDY #00
  E0 84 FE               STY FE
  E2 84 FF               STY FF
  E4 C6 FF     NEWPAGE:  DEC FF
  E6 A2 07     NEWBYTE:  LDX #07   ;bit counter
  E8 50 FE     LOOP:     BVC LOOP  ;wait for mono 3
  EA 2C 30 02            BIT 0230
  ED 18                  CLC
  EE 10 01               BPL SKIP
  F0 38                  SEC       ;set carry if mono
                                    2 was '1'
  F1 2A        SKIP:     ROL       ; form byte in acc.
  F2 CA                  DEX
  F3 10 F3               BPL LOOP  ;branch if word not
                                    complete
  F5 91 FE               STA (FE),Y ;store word in
                                    current mem loc.
  F7 C8                  INY       ;and move to next
                                    location
  F8 D0 EC               BNE NEWBYTE
  FA F0 E8               BEQ NEWPAGE
  FC DE FF reset vector = FFDE
```

Memory locations are loaded in the order FF00,FF01, . . FFFF, FE00,FE01... FEFF,FD00,FD01 etc

Implementations for other processors are just as simple. Good luck !

2650 LIBRARY

Having noted the introduction of **libraries** for the 8080 and 6800, and as no such library is yet available for the Signetics 2650, I thought I would offer my services.

I have a full set of the manufacturer's documentation, which is mainly hardware biased, but does include a couple of software items. As software is in such short supply any members (or otherwise) items would be most welcome.

Anyone requiring information please send a large SAE indicating requirements to Roger A Munt, 51 Beechwood Drive, Feniscowles, Blackburn, Lancs BB2 5AT tel; 0254 22341

9900 GROUP

I am interested in starting up a pool between people who have/have access to/are interested in the Texas Instruments TMS9900 microprocessor or minicomputer. Anyone interested, SAE please. Simon Garth 67 De Parys Ave., Bedford

PUZZLE ANSWER

Use Roman numerals and half them horizontally at a point equal to half the numerals' height. E.g. half of ten equals five; X cut in half = V

PUTATIVE PROM PROGRAMMER

H Comins

In the February issue of Byte, K B Welles describes a 'minimal' disk interface which relies on software for most of its logic. I thought that a similar approach would be useful in a PROM programmer. The design shown here is suited to the National MM1702, which I suspect is standard, but I can't be sure as I don't have any other programming instructions, although the Intel 1702 seems to be the same in other respects. It has the odd feature that the address has to be complemented half-way through the cycle, a capability very conveniently posessed by LCD drivers.

I'm afraid I'm not very knowledgeable about power supplies or high-voltage transistord, so the design is incomplete so far. If anyone is inspired to actually make one could they please inform me of their design for this part. The power requirements are 100mA at +12V, 10mA at -35V (20% duty cycle) & 300mA at -48V (20% duty cycle). The +12V and -48V must be current limited. Also a +5V supply is needed for the logic circuits.

A consideration of vital importance is how to be absolutely sure that -50V won't appear in the middle of your treasured computer. For a start we don't want to connect the PROM output pins to the data bus. Therefore I envisage having two pins on the programmer, one for programming and one for checking (The operation of the second one can be left to your imagination). In addition there is a 'power on' switch and a prompt light, which tells you when to switch it on & off. A final safety measure is to connect all input lines via a diods as shown in Fig 2 (the resistor is required for CMOS). For the power on flag the reverse arrangement can be used, but TTL requires a smallish pull-down resistor.

The operation of the program is as follows

User Instructions ; Turn off power switch, insert PROM, start program. When light flashes turn on power. Light will stay on. When it flashes again turn off power and remove PROM.

1 Reset all status bits. Execute loop to flash prompt light until 'power on' flag is set. Wait for supplies to stabilise.
2 Set address to 000. Turn on prompt light.
3 Set data to required pattern for current address.
4 Set address complement bit. Wait 25uSec.
5 Set DD/GG on bit. Wait 90uSec.
6 Reset address complement bit.
7 Set program pulse bit. Wait (say) 300uSec, or at most 3000uSec. Reset program pulse bit. Wait 10uSec.
8 Reset all status bits. Wait sufficiently long so that power supply duty cycle (DD and GG) is less than or equal to 20% (say 1700uSec).
9 Repeat 4 - 8 at least 32 times.
10 Increment address. If less than 377B return to 3
11 Flash prompt light until 'power on' flag is off.
12 Turn off prompt light and stop.

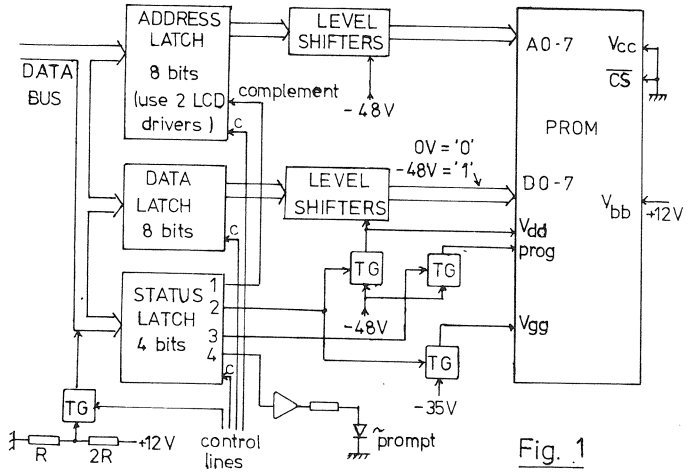


Fig. 1

TG = Transmission Gate

Status bits;
1 = address complement
2 = DD/GG on
3 = program pulse
4 = prompt

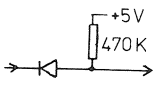


Fig. 2

KIT REVIEW

There are a number of kits now available which will allow the beginner to build up a -albeit limited - computer without needing an expensive teletype or VDU, instead they provide toggle switches or a small keyboard for data input and LED's or seven-segment displays for output. Programming must be done in machine language, usually in hexadecimal, but given the limited amount of memory available anyway, and the fact that some of these kits now allow program storage on cassette so that having created your program once you don't have to laboriously key it in every time you want to run it, the lack of a high level language need not be too insuperable a burden.

KIM-1 was probably the trend-setter in this area of low cost computing. It was reviewed in detail in Vol 4 Iss 4 of the ACCN, but the significant features are;6502 MPU. Teletype and cassette interfaces, 1.1k RAM useable by the programmer, and, they key feature, a 24 key keyboard (hex digits 0 - F plus some system controls) and hex displays for address and data, all running under the control of a system monitor in ROM. £185 from Transistor Devices Ltd.,Georgian House,Trinity St.,Dorchester. Memory expansion boards are now available.

Also using the 6502 MPU is the 'Data Handler' from Western Data Systems.(Europe via Romca Electronics B.V., Raadhuisstraat 4, Waspik, Holland, or SAE for details to 7 Dordells, Basildon, Essex).This board contains 1k RAM, LED displays for address & data, cassette interface option, and 26 keyboard switches (hex + control). It also features an output bus compatible with the S100 structure so that Altair/Imsai compatible boards can be added.

The 77-68 falls into this class - although not yet available as a complete kit-and RAM, monitor, I/O boards are being developed (watch this newsletter).

Rather similar to the 77-68, being based on the 6800 MPU and using toggle switches /LED's for primitive I/O, is the AMI-COS system from RITRO Electronics, Grengell Place, Maidenhead, Berkshire. A basic system, having the processor with 256 bytes of RAM and control panel costs £199. RAM, VDU and cassette interface boards will be introduced later.

Again using the 6800 MPU, there is of course the Motorola D2 kit, which comes as two boards, one holding the 6800 with 256 bytes of RAM, while a small (hex + control) keyboard and seven segment data/address display is on the other. The ROM monitor 'JBUG' includes a Kansas City compatible cassette interface. Bus buffers can be added to the processor board to make the system compatible with standard Motorola 'Exorciser' extension boards. About £190 from Marshall's,40-42 Cricklewood Broadway, London NW2 3ET.

Intel have just announced the SDK-85 kit which is based on their new 1.3uS 8085 MPU and has 256 bytes or RAM a programmable 14 bit timer, and numerous programmable I/O ports. a 2k byte ROM monitor drives the on-card 6 digit seven segment display and the 24 pad keyboard. An area of the board is reserved for adding extra components, such as bus buffers. The card will also interwork with a 20mA 110 baud teletypwriter. £187 from Rapid Recall Ltd, 11-15 Betterton St.,Drury Lane,London WC2H 9BS.

For those wanting to use the Z80 MPU,Cramer Components Ltd.,16 Uxbridge Rd.,Ealing,London W5 2BP sell the Zilog Z80 Kit for £230. This comprises the CPU with 256 bytes of RAM and a 1k byte monitor, cassette and TTY interfaces, 6 character seven-segment display, and (hex + control) keyboard, as well as a five slot motherboard. Memory and I/O expansion boards are available.

Finally, SC/MP'ers are served not only by SCRUMPI, which at £56 for an MPU with 256 bytes of RAM,LED display & toggle switch inputs must be the absolutely minimum system (Bywood Electronics, 68 Ebberns Rd, Hemel Hempstead, Herts HP3 9QRC) but also National's Introkit with 256 words of RAM plus a 512 word ROM monitor. This kit was designed to work with a teletypewriter, but the National keyboard kit will simulate enough to run the Introkit. About £132 the pair from Bywood or Marshalls.

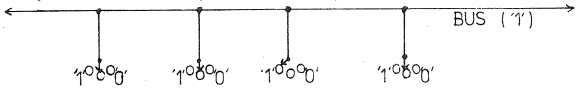
BUSSES *Part 3*

(Parts 1 & 2 were published in ACCN Vol 4)

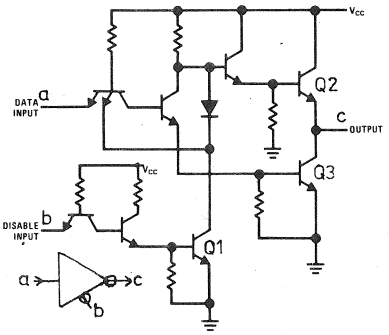
TRI-STATE BUSSES

The main disadvantage of the open-collector gate driven busses described previously is the relatively long time constant of the pull-up resistor / bus capacitance combination, which can easily add more than 100nS to the data transfer time (a long time when compared with the normal 10-20nS TTL gate delay). Also, useful drive capability is limited by the large current needed through the pull-up resistor to achieve a 'low' logic level.

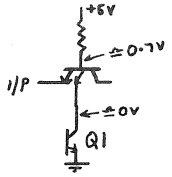
The solution to these problems was to design a bus driver with an output stage which, as well as being able to provide the normal '1' & '0' TTL levels, could also be turned off, to a 'high impedance' state. Then a number of these drivers could be connected to a common bus line, and as long as only one was enabled at any one time, all would be well;



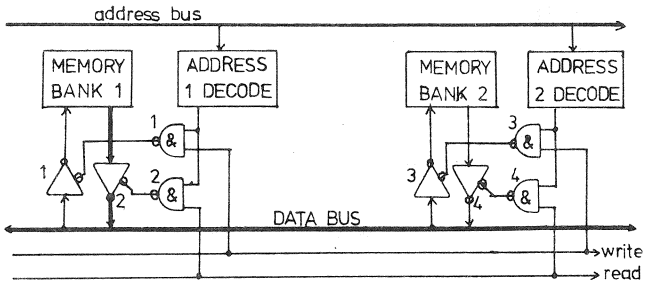
IC's having these characteristics were introduced by National Semiconductor in the late 1960's. A typical circuit is shown on the left. When the 'Disable' input is high (1), transistor Q1 turns on, and turns off both the output transistors Q2 & Q3. In practice some leakage current can still flow in Q2&3 (IX), but this is relatively small. The top half of the output stage (Q2 etc.) is designed to provide a higher current in the '1' state than is normal for TTL devices so that a satisfactory '1' voltage level can be achieved even when supplying the IX leakage currents of many driver output stages and also receiver inputs. Also, the higher '1' level output current gives a faster charge to the bus capacitances when going to the '1' logic level.



In the type of Tri-State gate shown, when Q1 turns on to turn off the output stage, it also effectively isolates the input line by pulling one of the emitters of the multi-emmitter input transistor to ground, so that the only input current which can flow into or out of the data input when the gate is disabled is a small leakage current IX. This feature enhances the use of this type of gate as a bus receiver, as if a large number of these inputs are connected to a bus line, the loading on the bus can be greatly reduced by de-selecting all of the inputs except those which are actually required at any instant. It should be noted, however, that this type of 'Tri-State Input' is not provided on all varieties of Tri-State gate or buffer, some, instead, have a 'low power' input which draws less input load current than normal TTL, but which is permanently in circuit.



A typical application of the type of Tri-State gate shown on the left is given below. Two memory banks are to be connected to a Tri-State data bus according to an address (on an address bus) and the state of the 'Read' & 'Write' lines. Thus, for example, if the address is such as to select mem bank 1, and the 'Read' signal is asserted, then the NAND gate 2 will give a '0' output, enabling buffer 2 to feed data from the memory onto the data bus, while Tri-State buffers 1,3 &4 will all be high impedance.




```
                                        Addr      Code
FMULT:  MOV MPCAND,SMPCAND              003   210 077 105
        MOV MPCAND+001,SMPCAND+001      006   210 100 106
        CLA PRODUCT                     011   040 102
        CLA PRODUCT+001                 013   040 103
        MOV #007,BITCNT                 015   050 007 104
        SHR MPLIER                      020   046 101
        GCC SHL1                        022   037 032
        MOV MPCAND,PRODUCT              024   210 077 102
        MOV MPCAND+001,PRODUCT+001      027   210 100 103
SHL1:   SHL SMPCAND                     032   047 105
        GTO SHL2                        034   030 041
ERR:    HLT                             036   000
        GTO ERR                         037   030 036
SHL2:   SHL SMPCAND+001                 041   047 106
        GCC SHR2                        043   037 047
        INC SMPCAND                     045   041 105
SHR2:   SHR MPLIER                      047   046 101
        GCC CKCNT                       051   037 071
        ADD SMPCAND+001,PRODUCT+001     53    211 106 103
        GCC ADD2                        056   037 064
        INC PRODUCT                     060   041 102
        GCS ERR                         062   036 036
ADD2:   ADD SMPCAND,PRODUCT             064   211 105 102
        GCS ERR                         067   036 036
CKCNT:  DEC BITCNT                      071   042 104
        GNZ SHL1                        073   033 032
MULTRET:GTO RET4                        075   030 170
MPCAND: HLT                             077   000
        DEF #001                        100   001
MPLIER: DEF #002                        101   002
PRODUCT:HLT                             102   000
        HLT                             103   000
BITCNT: HLT                             104   000
SMPCAND:HLT                             105   000
        HLT                             106   000
```

WB CORNER

A Fast Multiply routine for the WB-1, modified to allow storage - storage instructions of the type MOV X,Y as page 12 of ACCN Vol 4 Iss 5. Don't forget that the PRODUCT,PRODUCT+1 combination must be corrected. Thus;

002 320 represents 00 000 010 11 010 000

0 0 1 3 2 0

i.e. decimal 720

It might be a useful tip to those hand-assembling to put all data areas at the front of the program (you'll notice I don't practice what I preach !). Most instructions reference data fields, and the addresses may be filled in as they are compiled. Also, most alterations to programs once they are in the machine will not require the definition of more data, so the minimum alteration to existing machine code occurs. If the data is at the end, program expansion will throw out all addresses.

G D Hayes

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